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EDITORIAL

This special issue of the Journal is devoted to the modelling problems of semiconductor electronics. Modelling is an essential part of all theoretical investigations, the initial step of any abstract thinking. Modelling is a bridge between the physical reality with its infinite complexity and our finite tools and finite overview.

Modelling, however, is always coupled with an other task: the simulation. Simulation shows how the modelled physical structures behave, how the modelled processes will be carried out. This explains the fact that most of the articles of this issue treat not only the modelling but the simulation aspects too.

Modelling is a task showing an enormous diversity. As many task to be solved so many modelling problems. The selection of articles in this issue tries to reflect this variety: physical modelling, memory fault modelling, process step modelling are all related to the matter.

The introductory paper "Trends in microelectronics – European perspectives" by B. Courtois and M. Kerecsen-Rencz gives a general overview of the topic. Beyond VLSI modelling and simulation the paper is dealing with the state-of-art of IC design and with its educational problems. A very informative presentation of the trends and perspectives in semiconductor microelectronics is given in this article.

The article "Modelling semiconductor memory faults" by Prof. A. J.van de Goor, who is a worldwide know expert of this subject, treats the theoretical backgrounds of any practical test procedure of semiconductor memories. For the memories of today's bit size, the deep analysis of the possible faults is indispensable in order to generate good, efficient test sequences.

The close relations of modelling. simulation and verification is illustrated by the article of P. Jonsson et al. The modelling and simulation of a power semiconductor structure is followed by a very sophisticated measuring procedure. The internal carrier distribution of the device is investigated both by calculation and by a special measuring technique.

As the physical sizes of the semiconductor devices decrease new physical phenomena and new modelling challenges appear. A good example is the MOS transistor: if the device is scaled down to the submicron sizes the carriers and the dopant ions cannot longer be considered as a continuum. The individual "path of life" of each particle can be followed with the help of a 3D Monte Carlo type modelling and simulation procedure. The paper of Prof. K. Tarnay et al. is dealing with this problem.

Electro-optical interactions in semiconductor devices is an important topic due to significant advances in optical communication. The paper by Prof. T. Berceli et al. presents a circuit model for illuminated MESFETs and a measuring procedure for determining the model parameters.

It was a real pleasure for me to act as the guest editor of this issue and to collect a number of valuable articles in the topics of my special interest. I would like to thank all authors for the fruitful cooperation.

V. SZÉKELY

Vladimir Székely received the electrical engineering degree from the Technical University of Budapest, in 1964. He joined the Department of Electron Devices of the Technical University of Budapest in 1964. Currently he is a full-time Professor and the Head of Department of Electron Devices of TUB. His first research area was the theory of Gunn devices. His later research interests are mainly in the area of computer aided design of integrated circuits, with particular emphasis on circuit simulation, thermal simulation, and device modelling He conducted the development of several CAD programs in the field of integrated circuit design and simulation. He has been engaged in investigation of thermal properties of semiconductor devices and integrated circuits for the last 15 years. This resulted in the development of novel thermal based IC elements and thermal IC simulator porgrams. His newest fields of activity are computer graphics and image processing. Dr. Székely has published his theoretical and practical results in more than 90 technical papers.

TRENDS IN MICROELECTRONICS – EUROPEAN PERSPECTIVES

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Trends in microelectronics fabrication technology and design, with special emphasis on CAD are discussed in the article. After giving an overview of the world tendencies the European trends and efforts are presented and a short review is given about the state of the art of microelectronics in the East-Central European countries.

1. INTRODUCTION

This article was inspired by the research that one of the present authors, B. Corutois has carried out for the request of the French National Space Center about hardware/software systems' development and their future trends. He has written a large document under the title of "CAD and Testing of ICs and Systems: Where are we going?" [3], about microelectronics future trends, which became a frequent topic of discussion of the authors — with special emphasis on the European trends. This article is based on the above mentioned document — supplemented with some East-Central European views.

2. TRENDS IN MICROELECTRONICS FABRICATION TECHNOLOGY

Fig 1. shows the actual and forcasted market share of the different microelectronic fabrication technologies [11]. According to this figure, despite of the fact that an increase is expected in the market share of GaAs and BiCMOS technologies from 1-1% to 2% and 5% respectively, CMOS remains the mainstream technology for the '90s.

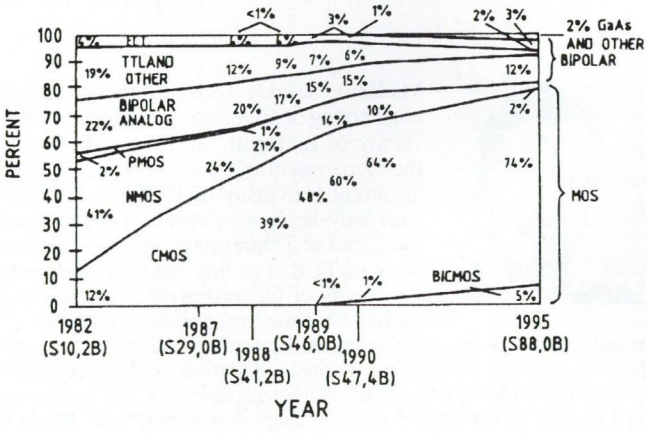

Fig. 1. Market shares of different microelectronics technologies [11]

BiCMOS, combining ECL bipolar performance with the high density and low power consumption of CMOS circuits is expected to become a strategic technology of the near future, and according to the prediction of Forward Concepts, resulting in the extinction of traditional bipolar products by the year 2000.

In the past a continuous decrease in the feature size characterized microelectronics development (Fig. 2.), and this tendency seems to characterize the whole decade [10]

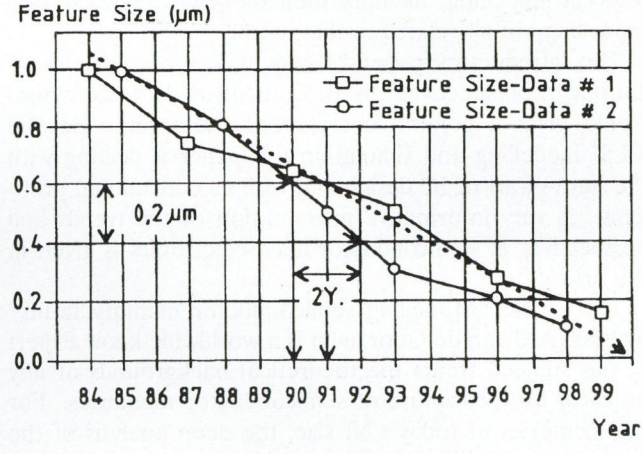

Fig. 2. Minimum feature size [10]

This is explained by the model developed by Maly:

- increasing the number of transistors by decreasing the feature size did not increase the cost (cost per transistor)
- increasing the chip size did increase the cost.

This is why WSI (Wafer Scale Integration) never became a mainstream technology. The model however predicts that the future might be different: instead of decreasing (as in the past), the cost per transistor might increase, by further decreasing the feature size. The exact point of time when this occurs is difficult to predict, but this is a big issue actually because of the exponentially increasing manufacturing costs [10], [8]. According to the invited address of H. Komiya (LSI Laboratory, Mitsubishi Electric Corp.) at the 40th ISSCC conference in San Fracisco, February 1993: "Technically feasible integrated circuit technology advacement may no longer be economically viable... wafer processing technology for feature size of $0.15\,\mu$, that would permit to reach 1 Gbit per chip may be available by the year 2000... on the other hand, ... simple extrapolation of trends in the past shows that research and development and production equipment investments for 1 G DRAMs will be 10–15 times and 30–40 times larger than those for 1M bit DRAMs, respectively..."

Facing this trend manufacturers enter alliances to share

the development costs and try to decrease the manufacturing costs by any means.

Users have alternatives to ULSI integration: they can use 3D (3 dimensional) packaging for memories and MCMs (Multi chip modules) for other products.

3. TRENDS IN MICROELECTRONICS DESIGN

3.1. Move from 5V to 3V

The transition from 5V bias voltage era to the 3V (3.3V, precisely) has started already. The driving force is the necessity to decrease power consumption, especially in the case of submicron circuits. Commercial circuits are already available with 3.3V bias voltage, however their performance is still worse than that of the 5V circuits (e.g. speed). An important research task of the next future is to find solutions for the analog functions which are suffering from lower voltages — in particular below 0.5 μ line widths.

3.2. Analog, mixed signal, digitized-analog ICs

According to Norton [14], the number of pure analog circuits would be rather decreasing than increasing, but the ratio of "digitized" analog circuits is growing. "Digitized" analog circuits include analog functions performed by digital, or mostly digital circuits. This is an approach that employs digital circuitry instead of analog circuits. It often implements new functions that could be performed neither by purely analog nor by purely digital circuits. On the other hand there is a growing trend towards embedding analog functions in digital chips, where such functions never existed before: microcontrolles, for example, now frequently contain embedded analog-to-digital or digital-to analog converter circuits.

3.3. FPGAs

Field Programmable Gate Arrays (FPGA) are used in the '90s for prototyping when fast specification checking is needed and for production when small quantities are required or when the specifications are expected to be modified. Their advantage — compared to the Mask Programmable Gate Arrays (MPGA) — is that they can be reprogrammed and can be fabricated by in-house processing for a relatively low cost in the case of small quantities. Their disadvantage is, however, the considerable lower operating speed and the much lower density. The total market of FPGAs is expected to grow from $160 million in 1991 to $1.66 billion in 1997.

3.4. Microsystems

The development of different kinds of sensors and actuators has raised the necessity to combine them with "intelligence", resulting in several kinds of micrsystems. A very important research field of the '90s is to find design and fabrication technological methods for sensors and actuators that are compatible with traditional microelectronics technologies resulting in a new, microsystem design and fabrication technology. Microsystems are expected to dominate automative, biomedical and some fields of home electronics applications for the end of the century.

4. TRENDS IN COMPUTER AIDED DESIGN

There have been 3 successive trends for CAD tools [1], [12], [13]:

- during the '70s: point tools, manufactured by CALMA, APPLICON, NCA, PDS...
- during the '80s: integrated tools manufactured by DAISY, MENTOR, VALID... and standards such as EDIF and CFI, allowing the transfer of data between different systems.
- during the '90s: automatic synthesis tools, user-design tasks interface, electro-mechanical integration, network systems...

Figures 3 and 4 depict the CAD world market in 1988 and in 1991.

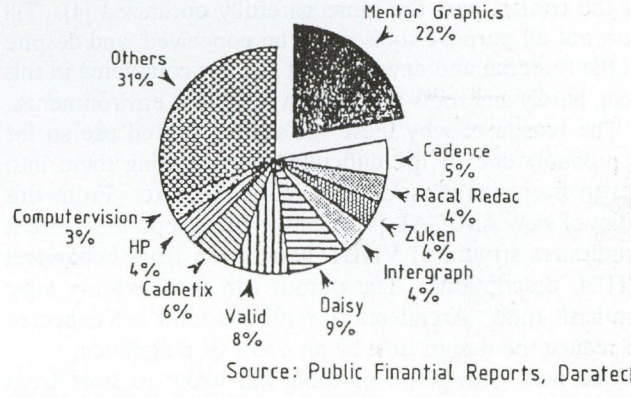

Fig. 3. Microelectrnics CAD world market in 1988

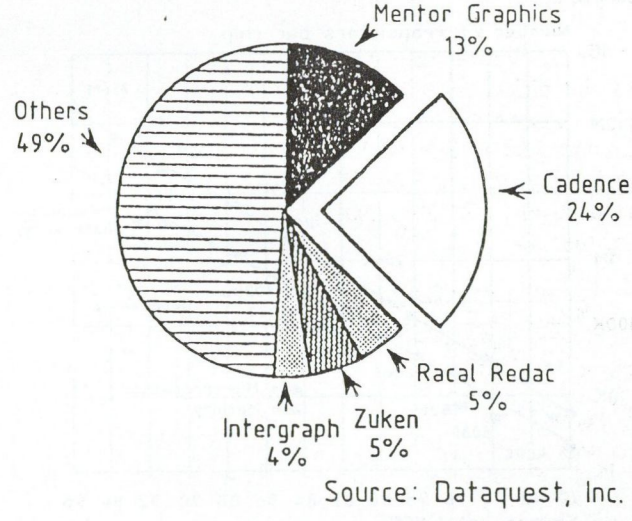

Fig. 4. Microelectrnics CAD world market in 1991

Fig. 4 shows the dominance of CADENCE — it has also won the university market. MENTOR GRAPHICS has lost the leading position that it had a few years ago, but it might recover. SYNOPSYS is the leading company in logic synthesis, they are said to have 1 or 2 years advace over their competitors. The main advantage of the SYNOPSYS system is that they could combine the

synthesis with the simulation and test environment, and their system enables switching from one technology to another without changing the description. VIEWLOGIC with its relatively cheap PC and workstation tools is expected to increase its market share in the near future [3].

The next generation of tools are the architectural synthesis tools. These tools will represent for archirecture what the SYNOPSYS system represents for logic. From a behavioral description they will enable architecture optimization — according to parameters such as area, performance, etc. The operation of these tools will be based on the intensive research carried out in this field since the '80s [6]. Several prototype systems were announced, mainly from universities. Most of these systems generate circuits consisting of a data-path and a control section. According to the type of application, either the parallelism of the data path or the complexity of the control part are more carefully optimized [4]. Till now not all purpose tools could be conceived, and despite of the research and development already completed in this field, hardly any tools are used in industrial environments.

The reason of why these tools have limited use so far is probably due to the difficulty of integrating them into design frameworks, such as CADENCE, etc. From this point of view AMICAL [9] seems to be exceptional since it synthesizes structural VHDL description from behavioral VHDL descriptions. The output can feed existing logic synthesis tools. Architectural synthesis tools are expected to reduce the design time by an order of magnitude.

The next generation of tools will allow to start from an even higher level — starting with hardware-software co-desing, partitioning, etc. [7]. This step is still under research.

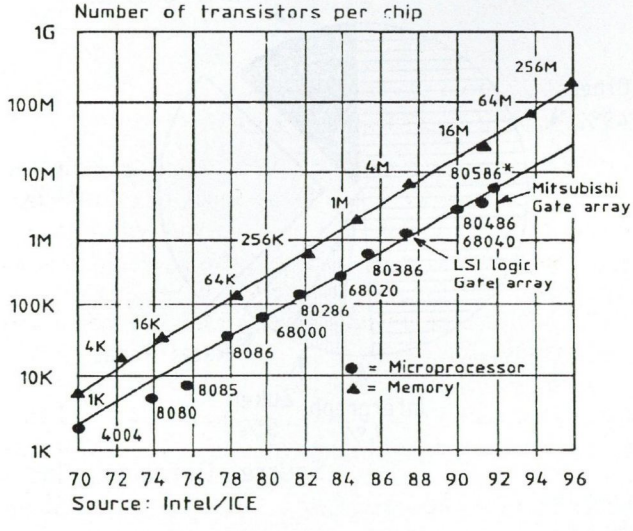

Fig. 5. Increase in IC complexity [3]

Research on CAD must address two key issues: productivity and innovation. Classical problems in IC design, like design rule checking, compaction, placement and routing, etc. are now largely solved, and slight improvements of existing algorithms are much less important than the gain in cost and performance obtained through the advance of hardware equipment. The cost/performance ratio of workstations has been continuously decreasing during the last years, so that only radical changes in the fabrication technology could require the development of new design algorithms.

The key issue is on design productivity.

According to Fig. 5 the complexity increase of memory and processor circuits continues to follow the increase rate of the last decades.

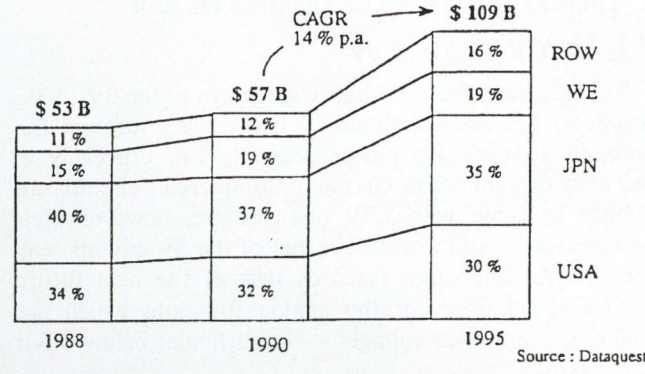

Fig. 6. Semiconductor consumption worldwide [3]

This predicts that the technology progress would allow a similar complexity increase of ASICs as well. DATAQEST indeed estimated the average number of gates in an ASIC for 25,000 in 1991, and an average design time of 8.1 months. In 1993 these figures should be 50,000 and 5.5 months: the average size of effectively designed ASICs then follows the rule of the increase of the maximum size, allowed by the technology progress. The above mentioned figures mean a production of 3,100 and 9,100 gates per month, respectively — in other words the need of multiplying the productivity by three in two years. It appears, however, that this need for productivity growth has not been satisfied up to now, since the number of designers allotted to a project increases [16], resulting in a clumsier design process and consequently in a loss in the relative design productivity.

According to H. de Man [5] the solution to increase innovation is to develop the new products together with their CAD tools; in a close association of an industrial team from the application sector, a research team (who formalizes and produces advanced CAD tools) and a small specialized CAD company (which manufactures operational tools to be implemented within the general tools produced by the major CAD companies).

5. EUROPEAN PERSPECTIVES

5.1. Industrial perspectives

Europe was not in a good position, compared to the US and Japan, as some well-known data remind us:

- while the US and Japan cover their respective demand production by "native companies", Europe continues to depend heavily on imports;
- the equipment market was rapidly shifting to Asia, with US companies losing production shares, while the Japanese was increasing and the European was remaining stable;
- Japan continues to dominate the worldwide semiconductor consumption (see Fig, 6);

- Japan dominates DRAMs and manufacturing equipment market.

Some signs however indicate a certain recovery of Europe:

- Europe's market share in worldwide semiconductors is expected to grow (see Fig. 7);
- Europe 's market share in worldwide electronics, that hardly increased from 1988 to 1990, is forecast to increase more significantly by 1995 (see Fig. 8);
- in semiconductor equipment sales, trends between the US and Japan have recently been reversed and a US company (Intel) became No. 1 again in 1992 in the semiconductor market. (Since 1987 Japanese companies owned this position).

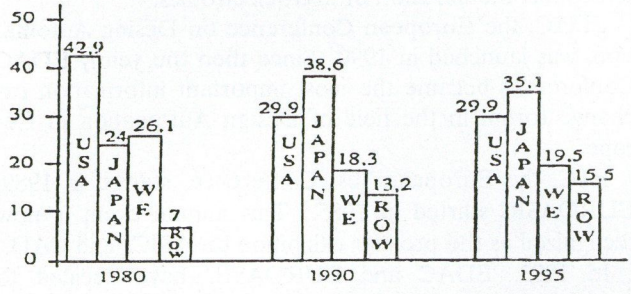

Fig. 7. Semiconductor market shares worldwide [3]

Microelectonics in particular, and Europe in general should benefit from the GRENOBLE 92 campaign and from GRESSI. GRENOBLE 92 is a SGS-THOMSON Microelectronics & FRANCE TELECOM-CNET (French National Center for Telecommunication) consortium. Started in 1989, this project (whose final cost will reach $ 600 million) consists of setting up a research and development line on 8" wafers (the first in Europe, operated by Europeans). The first .5 μ circuits were produced in August 1992 on the CNET research line. PHILIPS will participate in the development. The GRESSI (Grenoble Silicium Submicronique) association between CNET and the LETI laboratotry of the Nuclear Research Center of Grenoble will enable the development of research on more advaced technologies.

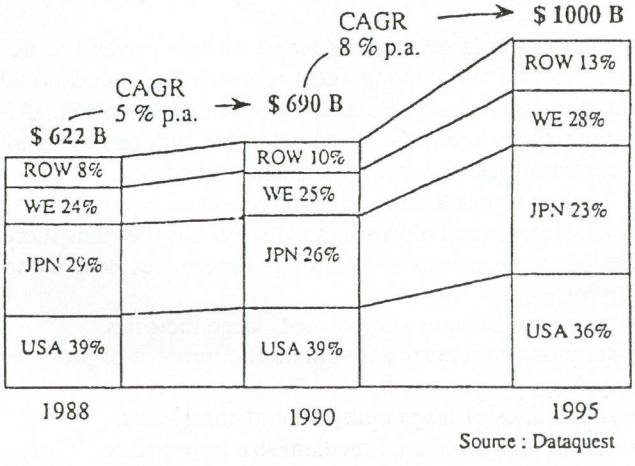

Fig. 8. Electronics market shares worldwide [3]

SGS-THOMSON Microelectronics has just benefited from a FF 1.2 billion recapitalization. French and Italian governments are in favor of a direct help to the microelectronics sector. In Germany, opinions are divided concerning the possibility of direct help as opposed to help for end-user sectors. A report from IFO (Institut für Wirtschaftsforschung) rejects the need for a direct help to semiconductor manufacturers, and recommends help for electronics users, claiming that these companies help circuit manufacturers by stimulating their sales in the end.

These two policies are not contradictory. They are the result of a weak vertical integration in Europe, particularly in France, compared with Japan for example. The heads of the JESSI (Joint European Submicron Silicon Initiative) program are strongly promoting a vertical integration. They actually managed to rebalance the program in favour of the Application sub-program (Automotive, HDTV, etc).

All these initiatives could make happen that Europe would be the winner of the third era, as projected by Vincent in [15]. The first era was the era of bipolar circuits needed by data processing systems, won by the USA in the 70s. The second era has been the MOS era, allowing large densities but less speed, won by Japan in the 80s. The emerging third era could be the era of smarter circuits like EPROM, flash, ASICs for complex function necessary for DSP, etc.. HDTV, automation, telecom industries will be giant application markets. Programs such as the ARIANE or AIRBUS programs give Europe strong positions in the corresponding sectors.

The European position is already strong in some fields: SGS-Thomson is world No. 2 in EPROM fabrication; PHILIPS and THOMSON are No. 3 and 4 in consumer electronics respectively, ALCATEL and SIEMENS among the 3 first in telecom, while BOSCH, MARELLI, VALEO, No. 1, 4 and 5 in automotive electronics.

5.2. Infrastructure

5.2.1. Promotion of EDA standards

To support European cooperation EDA standards are promoted in Europe by ECSI, the European CAD standardization initiative. ECSI is jointly sponsored by participating companies and the CEC via the ECIP (Electronic CAD Integration Project) ESPRIT project, and is open to all institutions or industries who wish to support EDA standardization in Europe.

It has the following aims:

- To help member companies to integrate new standards.
- To coordinate EDIF, VHDL, CFI and other standardization task forces.
- To increase visibility of Europe 's influence in standardization bodies.
- To issue and disseminate EDA standards information throughout EC countries.
- To provide input to the CEC and improve its policy towards EDA standards.

ECSI encompasses Technical Centers for VHDL, EDIF and CAD Framework areas.

There are VHDL Technical Centers at IMT, Marseilles and SIEMENS, Munich; there is an EDIF Technical Center at the University of Manchester; there is a EuroCFI

Technical Center at GMD, Bonn; and the ECIP office is based in Grenoble.

5.2.2. VLSI Education

In VLSI Education and Training, European Academic Institutions benefit from the VLSI Desing Training Action launched in 1989 by the CEC. EUROCHIP, a consortium of five Institutions (CMP in Grenoble, France, DTH in Lyngby, Denmark, GMD in Bonn, Germany, IMEC in Leuven, Belgium, RAL in Ditcot, United Kingdom) provides Academic Institutions with a number of services, including chip fabrication, procurement of industrial CAD software, procurement of hardware and testing equipment. EUROCHIP organizes courses in the use of basic CAD software, advanced training and the exchange of University CAD software as well.

Presently, 270 Academic Institutions from EC and EFTA countries participate in the Action and the scheme was recently opened to East-Central European coutries. Till now about 1,000 agreements have been concluded between EUROCHIP, Academic Institutions and industrial vendors and about 4,500 CAD software packages have been installed. 370 academic instructors have attended courses on the use of basic CAD software. More than 7,000 students have been trained in VLSI design during the first year of operation, and the figure went up to 10,000 for the second year. This is well beyond the initial goal: to double the number of yearly trained students within a few years, initially estimated to 3,000.

The high level of interest is also illustrated by the number of participants at the EUROCHIP Workshops held in Grenoble in 1991 and 1992: 300 and 400 respectively. No other scheme in the world has reached this level of service and this number of participating Universities [2].

Recently the scheme has been opened to cooperation between Universities and SMEs (Small and Medium size Enterprises).

5.2.3. Microelectronics service for SMEs

Innovative products nowadays often require an extra competitve edge through the application of microelectronics. Many SMEs are going in this direction. However, especially for SMEs, the route to VLSI is relatively expensive and bears a greater risk. In order to make VLSI more manageable for SMEs, the CEC launched in 1992 a new initiative: CHIPSHOP. CHIPSHOP is the Service Organizator of the JESSI-SMI Project, which plans to address 15% of an entire target group of 25,000 enterprises in Europe. CHIPSHOP will serve SMEs for chip fabrication and will link a network of support and competence centers (SCCs). Thus, design assistance and support can be given locally while prototype fabrication is performed on a European scale. CHIPSHOP offers more services besides prototype fabrication: testing, small volume production, CAD software, FPGA migration. The basic CHIPSHOP centers are SCME in The Netherlands, FhG-IIS and IAM in Germany, LETI and CMP in France, CNR-PF and CSATA in Italy, GAME and CNM in Spain, INESC in Portugal, INTRACOM in Greece, Electronikcentralen in Denmark and Norasic for the Scandinavian countries, ERA and ULVC for the UK.

The so called "Special Actions" were launched by the CEC to promote microelectronics in southern-European countries like Italy, Spain, Portugal and Greece. They are linked to JESSI-SMI via CHIPSHOP.

5.2.4. European conferences

However European Conferences exist for a long time on circuit desing and solid state circuits (ESSCIRC and ESSDERC) over the last five years Europe has launched several new European Conferences to strengthen the European infrastructure for education and research and to support the diffusion of microelectronics.

EDAC, the European Conference on Desing Automation, was launched in 1990. Since then the yearly EDAC Conferences became the most important information exchange forum in the field of Design Automation in Europe.

ETC, the European Test Conference, started in 1989. EUROASIC started in 1985. This annual event is now recognized as the premier exhibition on ASICs and CAD.

In 1993, EDAC and EUROASIC have decided to combine into a single Conference and Exhibition that has brought together ASIC designers and CAD users, developers, suppliers and researchers, resulting in the premier European Conference and Exhibition on Design Technology.

In 1994, EDAC, ETC, and EUROASIC have decided to combine into a single conference on Design and Test and an Exhibition that will bring ASIC and CAD companies together with CAT and ATE companies. EDAC-ETC-EUROASIC will be held in Paris in 1994.

Prototyping in general is becoming more and more crucial. The Rapid System Prototyping Workshop launched in 1990 in the USA will be held in Grenoble in 1994.

The yearly Workshop on CAD for VLSI in Europe (CAVE) exists already for 10 years, under the auspices of the CEC.

5.3. Microelectronics perspectives in Eastern-Central Europe

The following overview is based on the survey the authors carried out among their research and educational partners in Hungary, Poland, Estonia and Rumania. Although there seem to be considerable differences in all these countries, the main tendencies are similar.

The main problem in all these countries is the collapse of the state owned electronics industry. On the ruins there are four main groups of electronics enterprises strugling to survive

- privatized (former state owned) large factories,
- state owned enterprises with all the burdens of previous system,
- subsidiaries of large multinational companies,
- private new small and medium size enterprises.

The ratio and the weight of these four types differ in the former E/C European countries, but it is common in all of them that the biggest problems are the lack of

investment funds which would be needed to modernize the fabrication technologies, the lack of the solvent market and the lack of the marketing skills. In spite of all the expectations in the third group the work carried out in the E/C European countries is mainly assembling — the traditionally well trained electrical engineers of these countries do not find here enough creative work. Because of this, and because of the breakdown of the former large Research Istitutes, the SMEs (in the fields of the electronics, telecommunication, computing, etc.) are created mainly by electronic engineers — who have no managerial and marketing skills. In spite of this, this very flexible group of enterprises seems to be the most promising from the point of wiew of the survival of microelectronics in the E/C European countries. Some of them are growing very fast, and now have reached already the era of conceptional new developments.

The affordable price of FPGAs explains that the SMEs do not really suffer from the lack of the local microelectronics industry, and hopefully more and more will be able to benefit from the EEMCN (East European Microelectronics Cooperation Network) initiative, set up in the framework of the Cooperation in Science and Technology (PECO) program of the CEC to support ASIC design in E/C European countries, to build their equipment with up-to-date ASICs.

Although no competitive silicon foundry has survived in E/C Europe, the European educational cooperations (first of all the EUROCHIP cooperation, to which the E/C European countries could join informally 2, formally 1 year ago) enable the E/C European universities to keep their microelectronics education on the European standards. We consider this very important, since today VLSI design skills belong to the basic tool set of electronics engineering.

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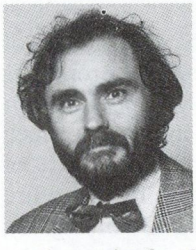

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MODELLING SEMICONDUCTOR MEMORY FAULTS

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This paper presents the functional model of (static) real-alterable memory (SRAM) chips. The main building blocks of the functional level are detailed at the electrical level. The classical functional fault models used for testing SRAM chips are introduced and their relationship between faults at the electrical and geometric level is shown. Inductive fault analysis techniques and empirical test date are used to show the relative frequency of occurrences of the introduced functional faults; and finally, references to march tests are given for detecting those faults.

1. INTRODUCTION

Memories are an important component in digital systems because they constitute a large percentage of the memory chips and, because of their high density, determine the system reliability to a very large extent.

The exponential increase in memory density (a quadrupling in density every π years) has obsoleted the traditional memory tests which required a test time of the order $O(n^2)$, where n is the number of memory bits in the chip. New fault models and memory tests have recently been designed such that memories can now be tested with tests requiring a test time of $O(n)$.

This paper starts with introducing the functional RAM chip model; in the next section, the main building blocks of this functional model are subsequently detailed at the electrical level. The currently used RAM chip fault models are described next; followed by a section which shows the validity of these fault models, using inductive fault analysis techniques and empirical test data. References are given for tests detecting faults of the described fault models.

2. THE FUNCTIONAL RAM CHIP MODEL

Fig. 1 shows a general model of a DRAM chip; for a SRAM chip the refresh logic would be omitted. Before discussing Fig. 1 in detail, one should be aware of the difference in the external and internal organization of the memory cell array D. A 1 Mbit chip may *logically* (as seen from the outside) be organized as 1M addresses of words which are one bit wide. *Physically* (inside the chip), the memory cells (each of which contain one bit of data) are organized as a matrix or a number of matrices. For example, the physical organization could be a matrix of 1k·1k bits (1k rows and 1k bits per row), or four matrices of $512 \cdot 512$, or 8 matrices of 128·1k, etc. For every read and write operation, a 1 kbit (or smaller) *row* is read or written internally, while only one bit is made visible to the outside world.

Block A, the address latch, contains the address. The high-order bits of the address are connected to the *row decoder*, B, which selects a row in the memory cell array, D. The low-order address bits go to the *column decoder*, C, which selects the required columns.

When the read/write line indicates a read operation, the contents of the selected cells in the memory cell array are amplified by the sense amplifiers, F, loaded into the data register, G, and presented on the data-out line(s). During a write operation the data on the data-in line(s) are loaded into the data register and written into the memory cell array through the write driver, E.

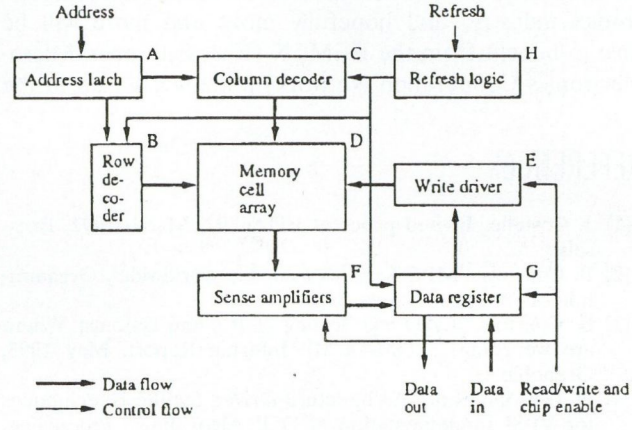


Fig. 1. Functional model (data path and control) of a DRAM chip

In the chip of Fig. 1, many different faults can occur. Fig. 2 lists some functional faults (at the electrical level) that can occur in a RAM chip (the list is not complete!). In the figure the following terminology is used: a *cell* is a device that contains data, like a memory cell or a cell in a register; and a *line* is a connection, it is used to transmit data or a control signal from one block to another or within a block.

3. THE ELECTRICAL RAM CHIP MODEL

The most important blocks of the functional model of Fig. 1 will be opened, such that the electrical properties of those blocks will become visible. This is important for a later explanation of the reduced functional faults, which have their origin at the electrical or geometrical level of the system. This section covers: memory cells (these are used to construct the memory cell array, D, of Fig. 1), decoders (used to construct the row decoder, B, and the column decoder, C), and the read/write circuitry (blocks H and F).

3.1. Memory cells

A **six-device SRAM cell** is shown in Fig. 3. It consists of the enhancement mode NMOS transistors Q_1, Q_2, Q_5

and Q_6; and the depletion mode NMOS transistors Q_3 and Q_4. Transistor Q_1 forms an inverter together with depletion load device Q_3, this inverter is cross-coupled with the inverter formed by Q_2 and Q_4, thus forming a *latch*. This latch can be accessed, for read and write operations, via the *pass transistors* Q_5 and Q_6.

	Functional fault
a	Cell[a] stuck
b	Driver stuck
c	Read/write line stuck
d	Chip-select line stuck
e	Data line stuck
f	Open in data line
g	Short between data lines
h	Crosstalk between data lines
i	Address line stuck
j	Open in address line
k	Shorts between address lines
l	Open decoder
m	Wrong access
n	Multiple access
o	Cell[a] can be set to 0 but not to 1 (or vice-versa)
p	Pattern sensitive interaction between cells[a]

[a] A cell can be a cell in the memory cell array or in the data register.

Fig. 2. List of functional faults

The addressing of the cell is done using a two-dimensional addressing scheme consisting of a row and a column address. The row decoder, B, of Fig. 1 allows only one row of cells to be selected at a time by activating the *word line* (WL) of that particular row (note that within the chip a memory word is synonymous with a row). The WL is connected to all gates of the pass transistors of all cells in that row, and only one WL should be active at a time. The selection of a particular cell in a row is done under control of the column decoder, C, of Fig. 1; it activates the set of complementary *bit lines* (BLs) of that particular cell.

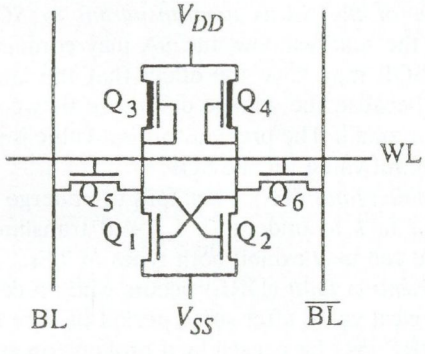


Fig. 3. Six-device SRAM cell structure

Data can be written by driving WL high and driving the lines BL and $\overline{BL}$ with data with complementary values. Because the bit lines are driven with more force than the force with which the cell retains its information (the transistors driving the lines BL and $\overline{BL}$ are more powerful, i.e. they are larger than the transistors Q_1 and Q_2), the cell will be forced to the state presented on the lines BL and $\overline{BL}$. In the case of a read operation, a particular row is selected by activating the corresponding WL. The contents of the cells on a row, accessed by the activated WL , are passed to the corresponding sense amplifiers via the BL and $\overline{BL}$ lines. The data register, D, of Fig. 1 is loaded by selecting the outputs of the desired sense amplifiers under control of the column decoder, C.

3.2. Decoders

Decoders are used to access a particular cell, or a group of cells, in the memory cell array. A 1 Mbit chip, externally organized as 1M addresses of 1-bit words, would require 1M word lines. The silicon area required for the decoder and for the word lines would be prohibitive. Therefore two-dimensional addressing schemes are used within the chip, requiring a row decoder with word lines (WLs) and a column decoder with bit lines (BLs); the size of each decoder and the area required for the lines is proportional to $\sqrt{n}$, where n is the total number of bits in the chip.

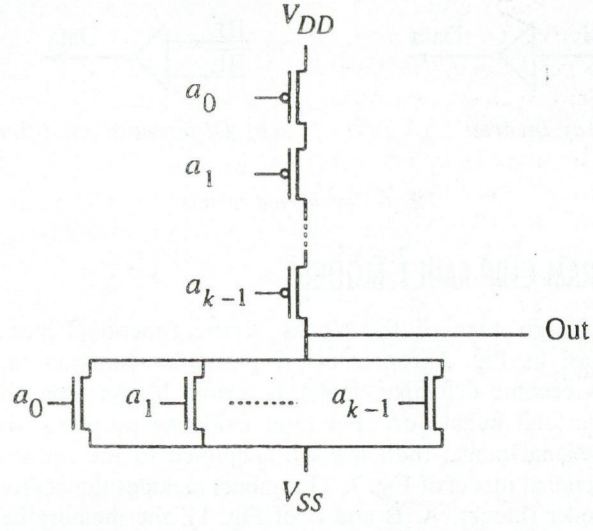


Fig. 4. Static row decoder circuit

An implementation of a simple, *static row decoder* consists of a NOR gate, as shown in Fig. 4. The inputs to the decoder consist of the address bits a_0 through a_{k-1} or their complements; the output (Out) is the WL line in case of a row decoder, or the CL (column select) line in case of a column decoder. All inputs a_0 through a_{k-1} have to be low in order for the output to be high. When a particular address has to be selected, e.g. address 50, which is 110010 in binary, the inputs to gates a_0 through a_5 should be as follows: $\overline{a}_0\overline{a}_1 a_2 a_3 \overline{a}_4 a_5$. For a large number of address lines, this decoder may become slow because of the long series of PMOS transistors in the V_{DD} path.

3.3. Read/write circuitry

The write circuitry of a RAM cell is rather simple; for an example, see Fig. 5. The to be written data on 'Data In' is presented on the BL and $\overline{BL}$ lines under control of the 'Write' clock.

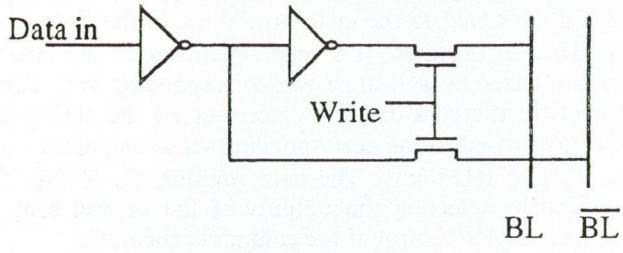


Fig. 5. RAM write circuit

The read circuitry may be very simple for ROM-type memories and small SRAMs. Fig. 6(a) shows a simple read circuit, consisting of an inverter. Fig. 6(b) shows a differential amplifier which can sense small differences between the lines BL and $\overline{BL}$ and allows for fast switching; read circuits are therefore also called **sense amplifiers.** The amplifier is enabled by a column select line, CL. The most common implementation of the read circuit for a DRAM cell consists of a sense amplifier implementation called *gated flip-flop* (Dillinger, 1988).

(a) Inverter *(b) Differential amplifier*

Fig. 6. Simple read circuits

4. RAM CHIP FAULT MODELS

Though each of the blocks of the functional model shown in Fig. 1 represents a particular function and may become defective, faults in certain blocks show the same fault behaviour. For fault modeling purposes, the functional model then may be simplified to the reduced functional model of Fig. 7. This model includes the address decoder (blocks, A, B and C of Fig. 1), the memory cell array, and the read/write logic (blocks E, F and G of Fig. 1).

Faults in the address decoder. Address decoder faults (AFs) are assumed not to change the decoder into sequential logic and be the same during read and write operations. Fig. 8 shows the functional faults that can occur in the address decoder. They are:

- *Fault 1.* With a certain address, no cell will be accessed.
- *Fault 2.* A certain cell will not be accessible.
- *Fault 3.* With a certain address, multiple cells are accessed simultaneously.
- *Fault 4.* A certain cell can be accessed with multiple addresses.

Faults in the memory cell array. Many different faults can occur in a memory cell array (van de Goor, 1990& 1991). These can be classified as faults which involve only a single cell (such as stuck-at, stuck-open, transition, data retention faults; and faults whereby a cell or group of cells influences the behaviour of another cell. The latter class is called coupling faults (CFs). CFs can be divided into inversion, idempotent, and state coupling faults. Also, CFs may be linked.

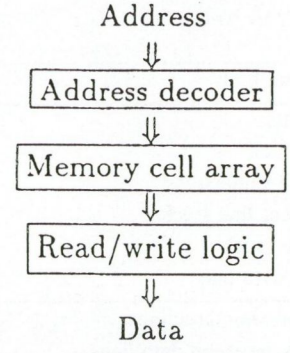


Fig. 7. Reduced functional SRAM chip model

In a *stuck-at fault* (SAF), the logic value of a stuck-at cell or line is always 0 (an SA0 fault) or always 1 (an SA1 fault).

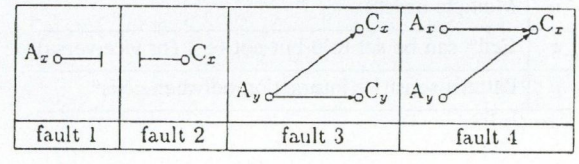


Fig. 8. Address decoder faults

A *stuck-open fault* (SOF) means that a cell cannot be accessed, perhaps because of an open word line (WL), see Fig. 8 (Dekker, 1990). When a read operation is performed on a cell, the differential sense amplifier has to sense a voltage difference between the bit lines (BL and $\overline{BL}$) of that cell. In case of an SOF, both bit lines will have the same voltage level; consequently the output value produced by the sense amplifier (SA) depends on the way it is implemented:

- *Operation of the SA is transparant to SAFs.* When the SA has only a single input (it is implemented as a buffer rather than a differential amplifier), an SOF will produce a fixed output value (always a 0 or always a 1). The SOF will appear as a SAF and therefore is detectable.
- *Operation of the SA is nontransparant to SOFs.* To broaden the read window, the SA may contain a latch. Then a SOF may have the effect that the latch is not updated because the voltage difference between the bit lines is too small. The previous output value is produced as the output value for the SOF.

In a *transition fault* (TF), a cell fails to undergo a $0 \rightarrow 1$ transition or fails to undergo a $1 \rightarrow 0$ transition. Note that a signal cell may exhibit both types of TFs.

A *data retention fault* (DRF) occurs when a cell fails to retain its logical value after some period of time (Dekker, 1990). A DRF may be caused by a broken (open) pull-up device within a cell (see Fig. 3). Leakage currents then will cause the node with the broken pull-up device to lose its

charge, causing a loss of information if a logic value was stored in the cell which required a high voltage at the open node.

An *inversion coupling fault* (CFin) (Nair, 1978; Suk, 1981; Marinescu, 1981) involves two cells i and j; the fault is sensitized by a transition write operation (that is an $\uparrow$ or a $\downarrow$ write operation) to a particular cell j. Cell j is called the *coupling cell*, and inverts the contents of cell i, which is called the *coupled cell*. Two different CFins can be recognized: the $<\uparrow;\updownarrow>$ and the $<\downarrow;\updownarrow>$ CFins. Between a given pair of cells i and j, both faults may exist simultaneously.

An *idempotent coupling fault* (CFid) (Nair, 1978; Suk, 1981; Marinescu, 1981) involves two cells i and j. The fault is sensitized by a transition write operation to a cell j, which forces the contents of another cell i to a fixed value (0 or 1). Four different CFids can be recognized: $<\uparrow;0>$, $<\uparrow;1>$, $<\downarrow;0>$, and $<\downarrow;1>$.

A *state coupling fault* (CFst) (Dekker, 1990) differs form the CFin and CFid because it is not sensitized by a transition write operation in the coupling cell but by some connection between two cells or lines. It is defined as follows: a coupled cell or line i is forced to a certain value x only if the coupling cell or line j is in a given state y.

Linked faults (Van de Goor, 1990& 1991; Parachristou, 1985) affect the same cell. In linked CFs, two or more CFs exist with the same coupled cell. Unless special precautions are taken in a test, fault masking may occur with linked faults. In fault masking, the fault effect disappears because when sensitized by one fault it is canceled by another fault.

5. VALIDITY OF THE FAULT MODELS

Tests can detect the presence of (reduced) functional faults, but they take time and therefore money. Currently, testing accounts for about half the cost of memory chips, so tests should only be performed to detect those faults which are reasonably likely to occur. The likelihood for a particular fault depends on the technology used, the feature width, the circuit design and layout, and the variations in the manufacturing process of a particular chip. This likelihood varies between chips of different manufacturers and even between chips manufactured in the same batch. We can use inductive fault analysis or physical defect analysis to determine this likelihood. In addition, the relationship between the faults at the *electrical* and *functional* level is established.

5.1. Inductive fault analysis (IFA)

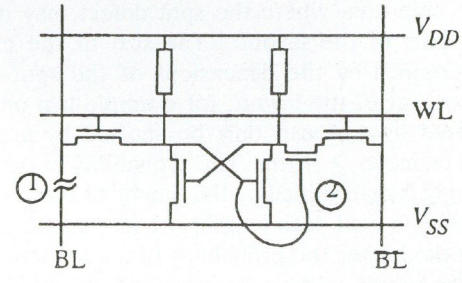
IFA is a systematic procedure to predict all faults (defects) likely to occur in an integrated circuit. The effect of each defect can be translated into one or more of the functional faults. The IFA method consists of inserting physical defects into the layout of a chip. Two classes of defects can be distinguished:

- *Global defects* may be caused by a too thick gate oxide, a too thin polysilicon, mask misalignments, and so forth. They affect many chips on a wafer and are the main cause of dynamic faults. Such faults are outside the scope of this article.
- *Local defects* (also called spot defects) are caused by extra, missing or inappropriate material (for example, dus particles). A spot defect affects only a single chip and causes a functional fault.

Dekker (1990) has investigated the effect of spot defects on 16-Kbit SRAM chips, manufactured with a 1.5-μm technology. He analyzed the effect of spot defects of different sizes for the memory cell array of the 16-Kbit SRAM chip. The spot defects then were translated into electrical faults, which in turn were translated into functional faults.

In (Dekker, 1987) 60 spot defects have been analyzed, starting with a translation from the layout to the electrical level; thereafter the resulting electrical faults are translated into logical faults. Fig. 9 (Dekker, 1990) shows how spot defect 1 is translated into an open bit line at the electrical level, while spot defect 2 is translated into an extra pass transistor. A few of the above faults will be explained, using Fig. 10 (Dekker, 1988); a complete analysis is given in (Dekker, 1987).

- *Fault 1*: a word line connected to V_{DD} will cause all cells along the word line to be stuck-open.



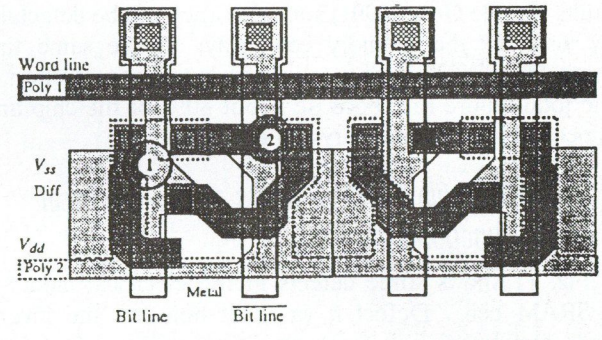


Fig. 9. Relationship spot defects — electrical faults

- *Fault 2*: a defect in the polysilicon layer covering a diffusion region may result in the creation of an extra pass-transistor, resulting in a TF.
- *Fault 3*: a cell node connected to a bit line will cause a CFst. If the node is low, all other cells on the same bit line will act as being stuck-at some value; if the node is high, all other cells on the sense bit line will function correctly.
- *Fault 4*: a broken pull-up resister will cause a data retention fault. If the cell is not accessed, the node with the broken pull-up resistor can be floating or active low. In case the node is floating, the leakage current from the cell node to the substrate will cause the voltage of

the node to drop; when the threshold voltage is reached the cell will invert. If the node is active low, the data retention fault is not present; hence the data retention fault is only detectable in one state of the cell.

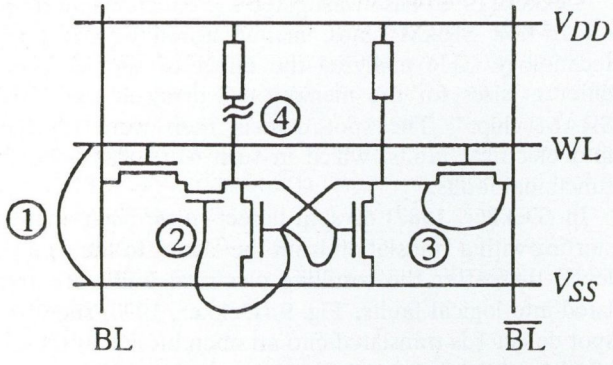


Fig. 10. Examples of defects in the electrical circuit

The importance, in terms of probability of occurrence, of the reduced functional faults of Section 4 caused by spot defects, depends on the critical area, which is defined as the chip area where the spot defect may damage the active part of the layout. The size of the critical area is determined by the dimensions of the spot defect and the topology of the layout; for example two parallel wires separated by 4 μ can only be shorted by a spot defect with a diameter ≥ 4 μm. The probability of occurrence of this short is determined by the lenght of the parallel wires, called the critical path length; the longer the critical path length the higher the probability of a spot defect.

Faults in the address decoder and the read/write logic have not been modeled by spot defects. The reason is that these faults can be mapped onto memory cell array faults (van de Goor, 1991) such that they will be detectable by tests for the memory cell array; at the same time these faults have a proportionally lower contribution to the total failure rate because about 80% of the chip area is occupied by the memory cell array.

5.2. Relationship between faults at the electrical and functional level

Fig. 11 shows some defects in the electrical model of a SRAM cell. Defect a (a short between the inverse node and V_{DD}) will result in a SA0 reduced functional fault. Defect b (a short between the true node and V_{SS}) will result in a SA0 fault. Defect c (an open, i.e. not connected, gate of the true node) will result in a SA0 fault.

Defect d (an open WL), will cause all cells after the WL to be inaccessible. When such a cell is read, the BL and $\overline{BL}$ lines will not be driven by the accessed cell because the pass transistors Q_5 and Q_6 do not conduct due to the open WL. The result of the read operation depends on the type of read circuit used, see Section 3.3; if the read circuit uses only one input (see Fig. 6(a)), the defect will manifest itself as a SA fault for all inaccessible cells; alternatively, if the read circuit consists of a differential amplifier (see Fig. 6(b)), it may be designed such that it will produce a fixed output value when both inputs have the same value (the defect will then also appear as a SA fault).

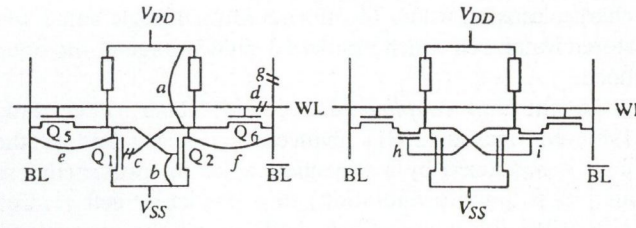


Fig. 11. Defects in a SRAM cell

Defect e (a short between the true node and BL) will have consequences if the cell contains a logic 0 value because defect e will pull BL down. If the cell contains a logic 1, BL will not be affected by defect e. The result of this defect is that all cells along the same BL will appear to be SA0 when the cell with defect e contains a 0; it can be considered the state coupling fault $< 0;0 >$. Defect f (a short between the inverse node and $\overline{BL}$) is similar to defect e; it will have consequences if the cell contains a logic 1. Then all cells along the same $\overline{BL}$ will appear to be SA1; this can be considered a state coupling fault.

Defect g (open $\overline{BL}$ line) means that the cells after the open defect will not be able to pass a logic 0 value on $\overline{BL}$. When a cell after the open defect contains a logic 0, it will be read correctly; when it contains a logic 1 value, the read result depends on the type of read circuit (see defect d).

Defects h and i show the creation of a news transistor due to faults in the polysilicon layer (Dekker, 1988). Given defect h and a logic 0 stored in the cell, the cell will be disconnected from BL; this will appear to be a transition fault, as will defect i.

Table 1.
Functional faults caused by spot defects

	Spot size	
Fault class	$< 2\mu$m (%)	$< 9\mu$m (%)
SAF	51.3	49.8
SOF	21.0	11.9
TF	0.0	7.0
CFst	9.9	13.2
CFid	0.0	3.3
DRF	17.8	14.8
Total	100.0	100.0

From Table 1, which shows the effects of spot defects on the memory cell array (which is 80% of the chip area), we can conclude that SAFs contribute about 50% to the total number of faults. CFins were not found, while TFs and CFids only occur with larger spot sizes.

5.3. Physical defect analysis

Dekker (1990) analyzed the physical defects in 1,192 defective devices from nine wafers, produced in three different batches, using a light microscope and a scanning electron micrograph. As shown in Table 2, the result shows

a large number of unidentified faults. Also, TFs hardly occurred, while SAFs account for about 60% and SOFs account for about 14% of the faults. In addition, CFids, CFsts and DRFs all did occur in practice. Note that the results of Table 1 (based on IFA) and of Table 2 (based on physical defect analysis) both show the occurrence of the same reduced functional faults (except for TFs), and that SAFs and SOFs are the dominant fault types.

Table 2
Validation of fault models

Devices (%)	Fault
59.9	SAF*
14.1	SOF
1.5	CFid
0.8	CFst
2.2	DRF
21.5	?

*Or total device failure

6. TESTS FOR SRAMS

Many types of tests for SRAMs have been proposed in the past. Currently, one family of tests, called **march tests**, has proven to be superior in terms of test time and simplicity of the algorithms. To detect all functional faults within a chip, one should test the address decoder, the memory cell array, and the read/write logic.

There are may march tests optimized for a particular set of functional faults. The three most important march tests are MATS+, March C-, and March B. Emperical results show the effectiveness of the proposed tests; for an overview see (van de Goor, 1993).

While these tests apply only to bit-wide memories, which allow only external access to a single bit, they can easily be extended to word-wide memories. Space limitations precluded discussion of DC and AC parametric tests, I_{DDQ} tests, and tests for (dynamic) recovery faults (for example, sense amplifier and write recovering faults). In addition, DRAMS require tests for neighbourhood pattern-sensitive faults (see van de Goor, 1991).

7. CONCLUSIONS

Functional fault models for (S)RAM chip have been established. Their origin at the electrical and geometrical level has been explained while, using inductive fault analysis techniques, of occurrence has been determined. $O(n)$ tests can be used to detect the faults of the described their relative frequency fault models; references to those tests are given.

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EVALUATION OF CARRIER IN POWER SEMICONDUCTORS USING BOTH OPTICAL AND ELECTRICAL MEASUREMENTS SUPPORTED BY TWO-DIMENSIONAL COMPUTER SIMULATION

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The ambipolar carrier lifetime in the n-base of a P-I-N type power diode has been extracted by using two independent measurement techniques, supported by appropriate computer simulations. Firstly, the *optical* free carrier absorption (FCA) method was used to measure the steady-state excess carrier distributions of the sample diode at different injection levels. Simulations with different carrier lifetimes were performed, and after fitting the simulated carrier concentration distributions to measured data an ambipolar lifetime of 20 ± 3 μs was achieved. Secondly, *electrical* reverse-recovery measurements were performed at both different current levels and reverse voltages. Simultaneously, computer simulations have been carried out in order to determine the recovered charge for different lifetimes, resulting in an ambipolar lifetime of 19 ± 2 μs. Furhtermore, measurements of an effective lifetime were done both with the open-circuit carrier decay (OCCD) method and the open-circuit voltage decay (OVCD) technique. The I-V characteristics were measured and simulated for different lifetimes, confirming an ambipolar lifetime of approximately 20 μs. Thsi work shows that the used simulation parameter models are close to reality and that the simulation results are reliable. The FCA method is also shown to be well calibrated.

1. INTRODUCTION

At Uppsala University we have a long tradition in physical modelling and simulation of semiconductor devices [1]. Computer simulation has become almost an everyday tool in the electrical/electronic design work during the past few years. With the easy access of commercially available physical simulation codes e.g. MEDICI [2], the demand on the simulation accuracy has also increased.

It is obvious, that simulations can only be as accurate as the models they are based on. In the case of physical simulation of semiconductors, stress is laid on the accuracy of the different physical parameter models in the equation system. The numerical analysis issues (robust solution algorithm, adequate discretization method etc.) are in most cases properly handled by the simulation software.

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Considering the behaviour of semocnductor power devices, recombination mechanisms play a central role among the simulated physical process. One should only consider that the trade-off between the on- and off-states bypol;ar power device could essentially improve with properly selected carrier lifetimes. Therefore, it is absolutely necessary to know real lifetime values for being able to do reliable simulations. A possible way is to make initial measurements, use these values as inputs to the simulation program, and iteratively compare the computed results with measured data.

In the literature, several attempts can be found for obtaining numerical parameters for computer simulations. Considering basic values (intrinsic carrier concentration, effective densities of state etc.) Green's paper [3] gives a good summary. For the carrier mobilities, one of the best recent papers is published by Klaasen [4]. In the field of power devices, electron-hole scattering plays an important role for the mobility models. This effect is often included into the mobility model see e.g. Dorkel and Leturq [5]. Regarding Auger recombination, an injection-dependent physical model, as obtained by electorluminescent measurements [6], is included in our calculations.

However, our main concern in this paper is to determine the Shockley-Reed-Hall (SRH) lifetime and to verify it through simulation. For this purpose, both electrical (reverse-recovery and open-circuit voltage decay, OVCD [7]) and optical (fee carrier absorption, FCA at steady-state [8] and open-circuit carrier decay, OCCD [9]) measurements have been performed. The obtained lifetime was used for the simulation of steady-state carrier distributions, I-V characteristics, and stored charge quantities/reverse-recovery times when the sample was driven with a given current ramp, see r.g. [10]. The simulated results were compared to corresponding measurements, giving a good agreement. The used samples, which were equvivalent in all respects, were electron irradiated power diodes.

The optical measurements, based on an infrared diagnostic method [8], are of special interest because they facilitate looking into the interior of a semiconductor device during its transient operational cycle. Infrared diagnostic methods based on recombination radiation or on the FCA

method have widely been used for performance analysis of silicon power diodes [11,12] and transistors [13].

The application of the FCA method for the analysis of thyristors was quite recently introduced [8,14]. Here, the FCA method uses a probing light beam from a HeNe lase in order to map the carrier distribution in a sample for steady-state conditions as well as for all phases of the transient cycles. The samples used for such measurements can be finger-cut parts from large-area thyristors, specifically preparated through polishing and etching. In this paper, however, P-I-N diode samples of similar shape are investigated.

2. EXPERIMENTAL TECHNIQUE

The FCA technique is based on low-energy photons illuminating a sample. The photons are associated with a wavelength ($\lambda = 3.39\ \mu m$) corresponding to an energy well below the bandgap energy of silicon, thus being scattered by mobile excess carriers in the material as well as by the material itself, see. Fig. 1. Hence, the radiation transmitted through the device without injected excess carriers, should be compared with the transmission values gives the local absorption coefficient, which entirely originates from mobile-carrier scattering. This absorption coefficient may be converted into the local excess-carrier concentration as a linear combination of the local electron and hole densities.

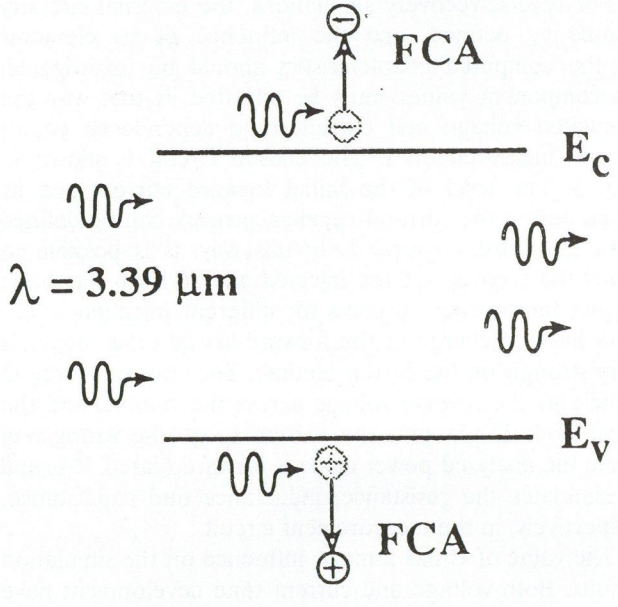

Fig. 1. Illustration of the physical principle of free-carrier absorption (FCA) measurements

The measurement system is shown schematically in Fig. 2. The system is composed by a low-power HeNe laser, a mechnical chopper for synchronization, beam-expander optics, a motorized positioning system with a pressurized sample holder which facilities scanning in two directions in a voltage-protective ambient, a focusing lens system, an amplifying photo-detector system, a digital wide-memory oscilloscope, and a computer.

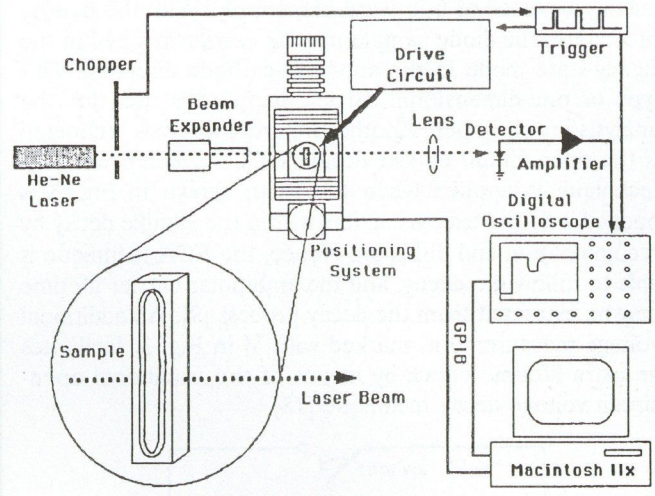

Fig. 2. Schematic view of the FCA measurement system

The diameter of the volume covered by the probing light spot is 30 μm, approximately, which sets the limit of the spatial resolution. The present FCA equipment facilities measurements of the turn-off process with a time resolution of approx. 500 ns. The high sensitivity of the equipmeent normally allows measurements of local carrier densities for a total device current density down to approximately 0.2 A/cm^2. An existive description of the instrument properties may be studied in [8].

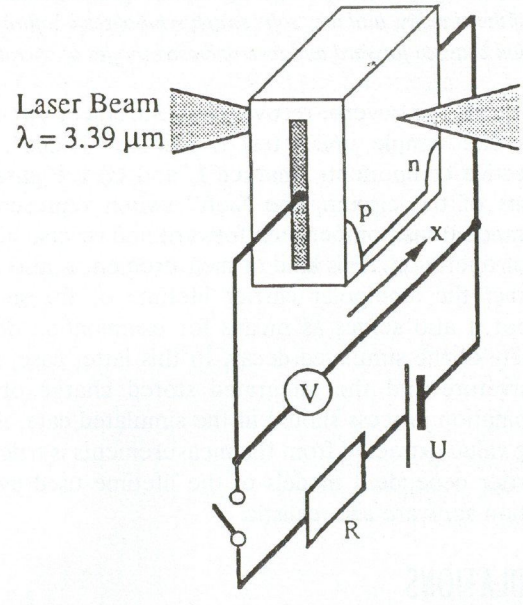

Fig. 3. Schematic view of the circuit used for FCA measurements of P-I-N diodes

In this paper, P-I-N diode samples were investigated by means of the FCA technique as well as by electrical measurements (reverse-recovery measurements). These measurements are well suited for the evaluation of the ambipolar carrier lifetime in the I-type base of the samples, in conjuction with appropriate computer simulations. Fig. 3 displays the circuitry for the FCA measurements of the P-I-N diode samples. A simple driving circuit was used, which

mainly consisted of a forward-bias supply. With this biasing procedure, the diode sample may be carrier mapped in the steady-state mode in the anode-to-cathode direction. This type of one-dimensional carrier mapping is used for the analysis in this paper. Another inherent analysis technique is the open-circuit carrier decay (OCCD) technique. This technique is applied when the swith shown in Fig. 3 is opened, and the excess carriers within the sample decay by recombination and diffusion, Hence, the FCA technique is able to follow the decay, and the ambipolar carrier lifetime may be extracted from the decay process [9]. An additional voltage measurement, marked with V in Fig. 3, facilitates an extra lifetime check by means of the traditional open-circuit voltage decay technique [15].

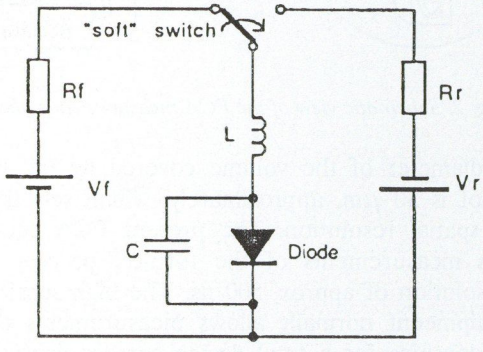

Fig. 4. The circuitry used for reverse-recovery measurements of P-I-N diodes. The reactive components (L and C) represent parasitic effects of the circuitry, and the "soft" switch symbolizes a soft/ramped transition between forward and reverse biased modes of operation.

In Fig. 4, the reverse-recovery measurement circuit is shown. The sample under test is marked "Diode", and the reactive components (marked L and C) are parasitic elements of the circuit. The "soft" switch represents a soft/ramped transition between forward and reverse biased mode of operation. This kind of measurement is also used to extract the ambipolar carrier lifetime of the sample base, but it also serves as means for examination of the credibility of the simulated decay. In this latter case, both the curvature and the integrated stored charge of the recombination process should fit the simulated data, if the lifetime value extracted from the measurements is true and the carrier dependent models of the lifetime used by the simulation software are realistic.

4. SIMULATIONS

For computer simulations, two different programs have been used: BAMBI [16], and MEDICI [2]. Both programs are two-dimensional taransient simulation codes, and they have been made equivalent by us to a necessary physical model level. However, MEDICI has a more robust numerical algorithm and it also runs faster. In addition, MEDICI's physical model structure is rigid and no source code was available for us (when this invetisgation was done). Thus, it was onnly allowed to change certain parameters in the formulae. BAMBI, on the other hand, was more flexible in that sense, that its source code was available and necessary changes could easily be accomplished. BAMBI's drawback is that it only is able to handle a simple outer circuit around the analyzed device. This simple circuit was not enough to make the reverse-recovery investigations; for that purpose, MEDICI had to be used. However, for calculating I-V characteristics, the use of BAMBI was adequate and simple. Hence, the physical model descriptions, which are detailed in the following, are valid for both programs (the necessary MEDICI formulae have been coded and linked with BAMBI). Test have been made, proving that these two programs practically compute the same results, providing that the same input structure and physical models are used.

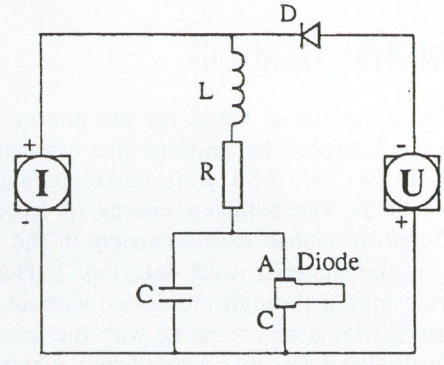

Fig. 5. The outer circuit used in simulation. Only one half of the sample structure is simulated, due to symmetry.

For reverse-recovery simulations, the external circuitry should be defined, and the influence of its elements to the computed characteristics should be investigated. Its component values must be adjusted in that way the simulated voltage and current time dependence equals to the measured ones. The chosen circuit is shown in Fig. 5. The level of the initial forward current and its slope during the turn-off ramping process can be defined with the current source I. In this way, is is possible to study the recovery of the injected charge from the diode during the transient process for different injection levels. This injected charge in the forward-biased diode depends very strongly on the carrier lifetime. The voltage source U generates the reverse voltage across the sample, and the ideal diode D prevents the current to go the wrong way while the analyzed power diode is forward biased. R,L and C simulates the resistance, inductance and capacitance, respectively, in the measurement circuit.

The value of C has a major influence on the simulation results. Both voltage and current time development have to fit measured data. If C decreases, the peak of the i(t) curve will move downwards, while the peak of the v(t) curve moves to the left, as is seen in Fig. 6. According to measurements, there is only a minor delay between the current and voltage peak. Hence, a set of C= 300 pF, L= 0.2 μH and R= 1 Ω is estimated in our case. The influence of the resistance and the inductance is, however, not very strong when looking at the displacement of the current and voltage peaks L almost only affects the magnitude of the megative voltage peak and the resistance acts as a moderator of the oscillations arising from the LC-circuit.

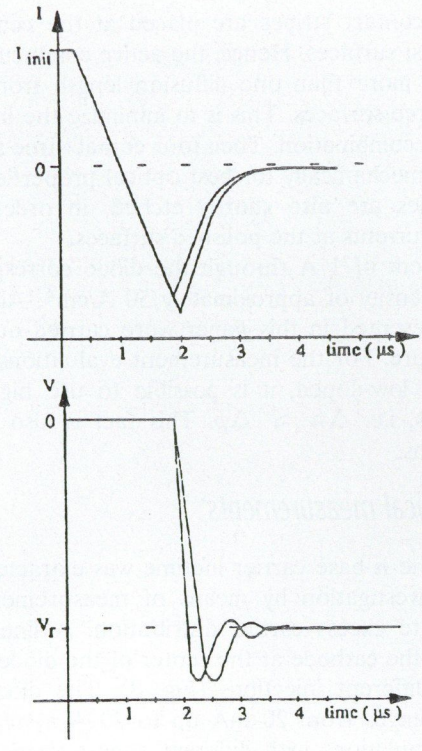

Fig. 6. a) Illustration of how the peak of the i(t) curve moves down if C decreases. b) Illustraion of how the peak of the v(t) curve moves sideways if C decreases.

Discussing the physical models used, MEDICI provides several choices for the mobility and lifetime models. The mobility models can generally be classified into three categories: low field, transverse field, and parallel field mobilities. For high−injecting P-I-N diodes, a low field carrier-carrier scattering mobility model was chosen. The effects of carrier-carrier scattering (C) are only important when high concentrations of electrons and holes are present. The model also takes into account the effects of lattice scattering (L) and ionized impurity scattering (I). The mobility model can be described by the following expression:

$$\mu_{0n,0p} = \mu^L_{n,p}\left[\frac{A.LIC}{1+\left[B.LIC\left(\frac{\mu^L_{n,p}}{\mu^{IC}_{n,p}}\right)\right]^{EX.LIC}} - C.LIC\right] \tag{1}$$

where A.LIC, B.LIC, C.LIC, and EX.LIC are all user accessible constans. For convenience, all MEDICI user accessible parametrs are written in CAPITALS. The term $\mu^{IC}_{n,p}$ is obtained from μ^C and $\mu^I_{n,p}$ according to Mathiessen's rule,

$$\mu^{IC}_{n,p} = \left[\frac{1}{\mu^C} + \frac{1}{\mu^I_{n,p}}\right]^{-1} \tag{2}$$

The carrier-carrier scattering term μ^C is given by the formula:

$$\mu^C = \frac{A.CCS(\frac{T}{300})^{3/2}}{\sqrt{np}ln(1+B.CCS(\frac{T}{300})^2(np)^{-1/3}} \tag{3}$$

The ionized impurity scattering terms μ^I_n and μ^I_p are given by the expressions:

$$\mu^I_n = \frac{AN.IIS(\frac{T}{300})^{3/2}}{N_T}\cdot g_B\left[\frac{BN.IIS(\frac{T}{300})^2}{n+p}\right] \tag{4a}$$

and

$$\mu^I_n = \frac{AP.IIS(\frac{T}{300})^{3/2}}{N_T}\cdot g_B\left[\frac{BP.IIS(\frac{T}{300})^2}{n+p}\right] \tag{4b}$$

where

$$g_B(x) = \left[ln(1+x) - \frac{x}{1+x}\right]^{-1} \tag{5}$$

Finally, the lattice scattering terms μ^L_n and μ^L_p are given by:

$$\mu^L_n = MUN0.LAT\left(\frac{T}{300}\right)^{-EXN.LAT} \tag{6a}$$

$$\mu^L_n = MUP0.LAT\left(\frac{T}{300}\right)^{-EXP.LAT} \tag{6b}$$

Electron and hole lifetimes used in MEDICI may be regarded concentration dependent in the simulation as follows:

$$\frac{TAUN0}{\tau_n(x,y)} = AN + BN\left(\frac{N_{total}(x,y)}{NSRHN}\right) + CN\left(\frac{N_{total}(x,y)}{NSRHN}\right)^{EN} \tag{7a}$$

$$\frac{TAUP0}{\tau_n(x,y)} = AP + BP\left(\frac{N_{total}(x,y)}{NSRHP}\right) + CP\left(\frac{N_{total}(x,y)}{NSRHP}\right)^{EP} \tag{7b}$$

where $N_{total}(x,y)$ is the local total impurity concentration and where $NSRHN$ and $NSRHP$ are properly chosen constant values. The values of $TAUN0$ and $TAUP0$ have been deducted from the measured ambipolar lifetime τ_0. Since our samples have been electron irradiated, the follwing holds [17]:

$$TAUN0 + TAUP0 = \tau_0 \tag{8}$$

$$\frac{TAUN0}{TAUP0} = 4.42 \tag{9}$$

The continuity equations for electrons and holes in MEDICI,

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla}\cdot\vec{J_n} - U_n = F_n(\Psi,n,p) \tag{10a}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\vec{\nabla}\cdot\vec{J_p} - U_p = F_p(\Psi,n,p) \tag{10b}$$

include U_n and U_p, which represent the net electron and hole recombination rates, respectively. MEDICI supports both Shockley-Reed-Hall and Auger recombination, i.e. $U = U_n = U_p = USRH + U_{Auger}$, where

$$U_{SRH} = \frac{pn - n^2_{ie}}{\tau_p\left[n + n_{ie}\exp(\frac{ETRAP}{kT})\right] + \tau_n\left[p + n_{ie}\exp(\frac{-ETRAP}{kT})\right]} \tag{11}$$

$$U_{Auger} = AUGN(pn^2 - nn_{ie}^2) + AUGP(np^2 - pn_{ie}^2) \quad (12)$$

Above, n_{ie} is the effective intrinsic concentration and τ_n and τ_p are the electron and hole lifetimes. The value of $ETRAP$ is the energy of active recombination centers, which may be measured by e.g. deep-level transient spectroscopy (DLTS).

Besides the recombination mechnaism described in the previous section, MEDICI also includes an extra recombination component at specific insulator-semiconductor interfaces, i.e. the SI-air and Si-SiO_2 interfaces. This recombination mechanism can be described by the surface recombination velocity. In MEDICI, surface recombination velocities for electrons and holes can be explicitly specified. For each node on a specific interface, an effective lifetime for each carrier type is computed (i.e. τ_n^{eff} and τ_p^{eff} using the given recombination velocities , S.N and S.P. Thus

$$\frac{1}{\tau_n^{eff}(i)} = \frac{S.Nd_i}{A_i} = \frac{1}{\tau_n(i)} \quad (13a)$$

$$\frac{1}{\tau_p^{eff}(i)} = \frac{S.Pd_i}{A_i} = \frac{1}{\tau_p(i)} \quad (13b)$$

where $\tau_n(i)$ and $\tau_p(i)$ are the regular SRH lifetimes at the node i. A_i is the semiconductor area and d_i is the lenght of the interface, both associated with the node i.

For BAMBI simulations of I-V curves, the power diode was simply driven by current-controlled boundary conditions in the appropriate current ranges. The used physical models were the same as those detailed for MEDICI.

4. MEASUREMENTS AND RESULTS

4.1. General remarks

The diode sample used for this investigation is a $p^+ - n^- - n^+$ (P-I-N) structure, with an n-base doping of approximately $3.5 \cdot 10^{13}$ cm^{-3}. The carrier lifetime is strongly reduced by means of electron irradiation with a dose of $5 \cdot 10^{12}$ cm^{-2}.

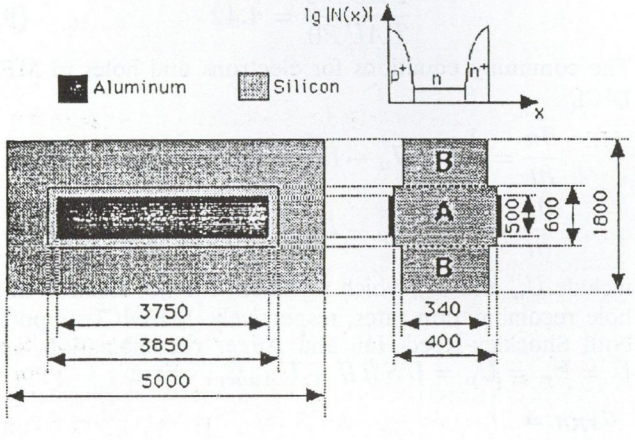

Fig. 7. Cross-sections of the sample diode. All dimensions are in μm.

The sample is cut to an appropriate size of about 0.25 × 2 × 5 mm (see Fig. 7). where the anode and cathode contact stripes are placed at the center of the two largest surfaces. Hence, the active conduction volume is placed more than one diffusion length from the four contact-free surfaces. This is to minimize the influence of surface recombination. Then four contact-free surface are polished mechanically for best optical properties possible. The diodes are also shortly etched, in order to avoid leakage currents at the polished surfaces.

A current of 1 A through the diode corresponds to a current density of approximately 50 A/cm^2. All measurements presented in this paper were carried out at room temperature. For the measurement evaluations, since the n-base is low-doped, it is possible to use high-injection conditions, i.e. $\Delta n \approx \Delta p$. This fact is also proven by simulations.

4.2. Optical measurements

First, the n-base carrier lifetime was extracted from an optical investigation by means of measurements of the steady-state excess carrier distribution. A line from the anode to the cathode at the center of the diode was scanned for different injections (Fig. 8). The diode forward current ranges from 20 mA up to 20 A at ten different levels. Simulations with different n-base carrier lifetimes were performed, and after fitting of the simulations to the measured data, an n-base carrier lifetime was achieved. The measured carrier distribution at steady-state are presented in Fig. 8, together with the simulated carrier distributions at the same corresponding currents. In this figure, the simulations were performed with an n-base lifetime of 20 μs, which gave the best fitting to the measurements.

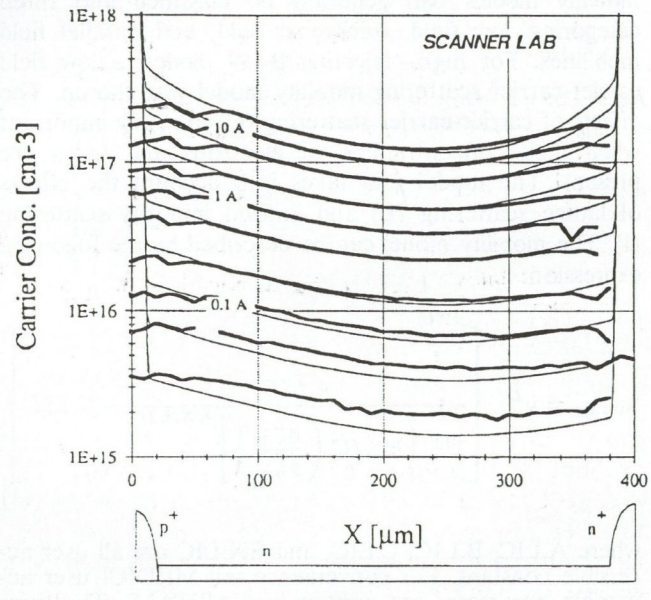

Fig. 8. Comparison between measured (thick lines) and simulated (thin lines) one-dimensional excess carrier distributions in the n-base of a P-I-N diode for different injection levels. The diode forward current ranges from 20 A (topmost two curves) to 20 mA (lowest two curves).

The optical measurements give absorption data, primarily. The measured absorption distribution then has to be converted into a carrier distribution. In this paper, the ca-

libration principle proposed by [18] has been used.

In Fig. 8 the simulations were carried out with an n-base lifetime of 20 μs. Simulations were, however, also carried out with 15 and 25 μs n-base lifetime. Furthermore, different levels of surface recombination velocities have been put into test in the simulation work. The simulated curves of Fig. 8 have been calculated with a surface recombination velocity of 10^4 cm/s, which is a common value for fairly rough surfaces that can be found in the literature [19]. Since the surfaces are polished and etched, the surface recombination velocity would be rather low. Hence, simulations with the lifetime of 20 μs were also made for no surface recombination at all, and in this case the curves fitted even better than in Fig. 8. These data, however, are not presented here, since a zero surface recombination velocity is rather non-physical, but they serve as an indication of an even lower surface recombination velocity than 10^4 cm/s.

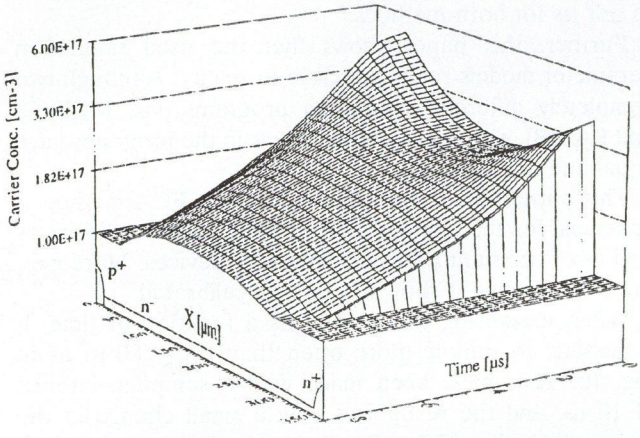

Fig. 9. Example of measured one-dimensional carrier distribution in the n-base of a P-I-N diode. The anode-to cathode carrier distribution is decaying from steady-state (at t = 0) to the open-circuit distribution after 8.8 µs. The forward current level is 20 A in this case.

As a minor part of this investigation, the OCCD technique [9] has been used to extract an effective lifetime. The closed circuit in Fig. 3 supplies a forward current to the sample diode, and when the circuit is broken the excess carriers are entirely diffused and recombined. A typical example of this shown in Fig. 9. With turn-off measurement data, like those in Fig. 9, the OCCD technique can be used to determine the ambipolar lifetime. This was done for all ten current levels. Scanning of the anode-to-cathode line through the diode was performed with 5 μm steps, whereas the spatial resolution of the FCA equipment is 30 μm. This procedure is equal to smoothing of measurement data, and is necessary since first- and second-order differentials of the data have to calculated in the OCCD technique, and these quantities are extremely sensitive to small errors and deviations.

The OCCD technique does take emitter recombination into account, but it does not deal with surface recombination in general. This is due to the lack of measurement data in the two direction towards the polished surfaces, and, hence, the diffusion in these two directions cannot be considered. There is, however, surface recombination present at the *anode and cathode sides* of the diode, and this is taken into account. Thus, the measure of the carrier lifetime will be correct of the surface recombination is negligbile. In these measurements, the surface recombination is most likely present, but not as a dominant limiter of the lifetime.

The optical measurements resulted in an n-base carrier lifetime of 20 $\pm$ 3 μs, whereas the OCCD-technique gave as result an *effective* lifetime of 15 μs$\pm$2 μs.

4.3. Electrical measurements

The second major part of this investigation was to perform electrical reverse-recovery measurements, and to compare them with computer simulations. By using not only a single method, e.g. the optical method, a more secured lifetime would be obtained.

The sample diode was first forward biased (Vf) through a resistance (Rf). After this, the circuit was broken and a reversed voltage (Vr) was applied. In this manner, the stored charge of the diode was pulled out, and a short reverse current peak was detected. The circuit used is schematically shown in Fig. 4. When integrating the reverse current peak in time, a charge is obtained. This charge is pronouncedly dependent on a) the forward current, b) the current slope when reversing the voltage, and, c) the carrier lifetime in the diode [10].

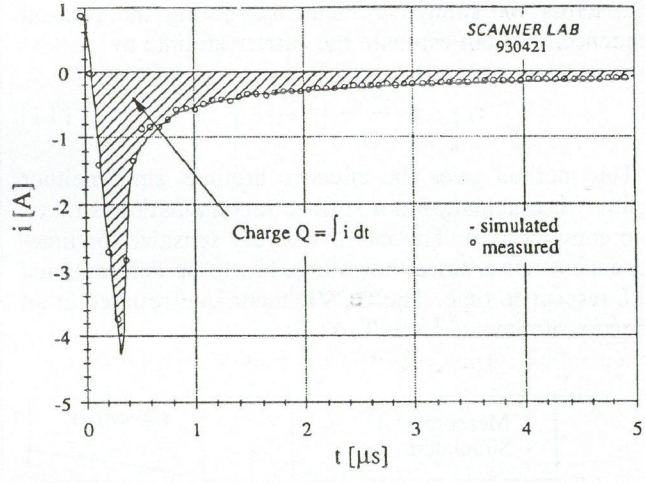

Fig. 10. Comparison between measured and simulated current of a ramped reverse-recovery process. The recovered charge Q is shown as the shaded area. In this particular case, the forward current is 1.0 A, the reverse voltage is 21 V, and the current slope is 16 A/µs.

Experiments were made at four different forward current levels, which all were in the same range as in the optical measurements, i.e. between 1 adn 10 A. Two different reverse voltages were used in order to achieve measurements at two different current slopes. The slopes were 16 and 100 A/μs, approximately. One measurements result is shown in Fig. 10 together with the corresponding time-resolved simulated current.

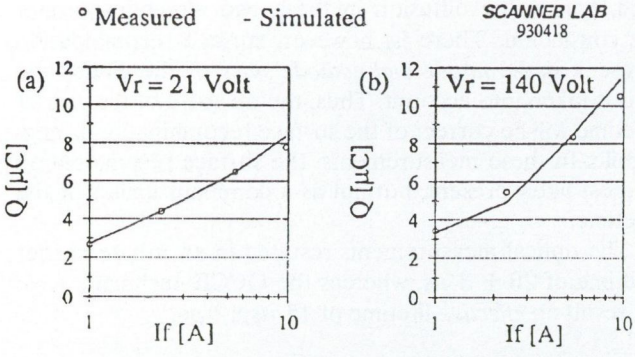

Fig. 11. Comparison between measured and simulated reverse-recovered charge for a P-I-N diode at four different forward current levels and at two different reverse voltages. The current slopes after turn-off are about 16 A/µs in (a) and approximately 100 A/µs in (b). In this simulation the n-base (bulk) lifetime used was 17 µs.

Simulations were carried out for n-base carrier lifetimes between 15 and 25 μs. In Fig. 11 measured charges and corresponding simulated charges are plotted. The measurements and the simulations in Fig. 11 agree very well, as well as the timing between simulated and measured currents in Fig. 10. These reverse-recovery experiments gave an n-base excess carrier lifetime of 19 ± 2 μs.

As another minor part, or as a check of the results, the carrier lifetime has also been estimated by using the well-known OCVD technique. If the open-circuit voltage V_{oc} across the sample is measured during the turn-off sequence, one can estimate the carrier lifetime by

$$\tau_{eff} = \frac{2kT}{q} \left(\frac{dV_{oc}}{dt} \right)^{-1} \qquad (14)$$

This method gives the effective lifetime, since neither emitter recombination nor surface recombination is taken into consideration. The method is very sensitive for time-dependent noise, since the voltage has to be differentiated with respect to time. The OCVD technique resulted in an effective lifetime of 13 ± 3 μs.

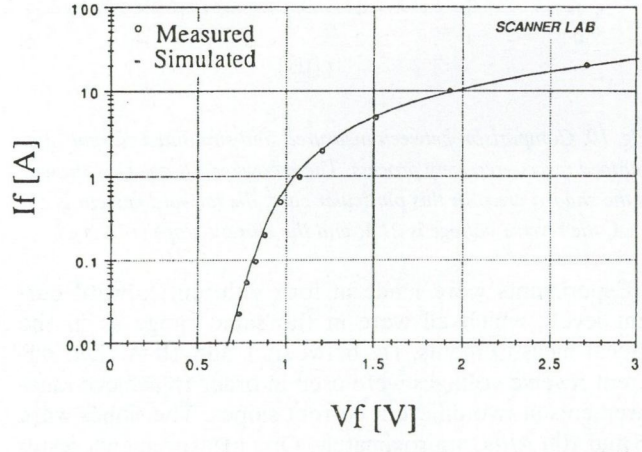

Fig. 12. I-V characteristics of a P-I-N diode. The simulated data (line) are compared with measured data (points).

The I-V characteristics of a diode is only weakly dependent on the bulk carrier lifetime. However, for the sake of completeness of this investigation, the I-V characteristics have been measured and simulated. The measurement was performed using a four-point measurement system at the same current levels as in the OCCD-measurements (i.e. 0.02 – 20 A), and the simulations were made for different n-base carrier lifetimes. The results are shown in Fig. 12, where the simulated I-V characteristics (curve) for a bulk lifetime of 20 μs coincides well with the measured (points). Thus, a lifetime of 20 μs in the sample diode appears to be a good estimate.

5. CONCLUSIONS

It is interesting to notice the good agreement between the two independent lifetime extraction methods, i.e. the optical and the electrical. The excess-carrier lifetime of the n-base of a certain electron-irradiated diode is determined to ± 3 μs for both methods.

Further, this paper shows that the used simulation parameter models really are close to reality. Although two completely different simulation programs, viz. MEDICI and BAMBI, were used, same models in the programs gave equal and reliable results.

This paper also shows that the optical FCA method is beneficial for the analysis of the steady-state conditions as well as of transient processes in power devices. Moreover, the FCA method is shown to be well calibrated.

When measuring the current as a function of time, it is possible to sample more often than every 80 ns as in Fig. 10. Tests have been made with a sampling interval of 10 ns, and the result was only a small change in the charge (less than 5%). On the other hand, the shorter the sampling interval chosen, the less of the whole current pulse cycle can be sampled. (It is necessary to measure the zero level before the forward current pulse, so that possible offset errors can be adjusted. You also must let the diode go into steady-state before it can be reversed. Then you must wait for the reverse current to decrease to as close to zero as possible.) Hence, the choice of the sampling interval and the sampling frequency has to be optimized.

There is, however, a small disagreement between measurements and simulations in the reverse-recovered charge for the highest current level. The simulations give a slightly higher value than the measurements. This trend has been observed in several experiments, and the explanation may lie in the value of the ambpolar Auger coefficient in the simulation program. A higher Auger coefficient than the used $16.6 \cdot 10^{-3}$ cm^6/s [20] would decrease the reverse-recovered charge at higher injections, since it would decrease the effective lifetime earlier, i.e. at lower injection levels, and thus decrease the stored charge. An Auger coefficient of $17.7 \cdot 10^{-31}$ cm^6/s as proposed by [6] has been tested, but the change in recovered charge was only marginal. Hence, a higher Auger coefficient probably will not eliminate the disagreement solely. It is, however, interesting to study the influence of the Auger coefficient on this behaviour in the future.

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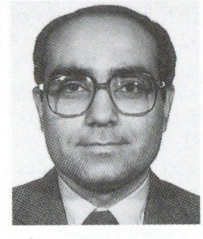

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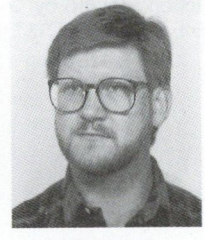

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EVALUATION AND INTERPRETATION 3D MONTE CARLO SIMULATION RESULTS OF SUBMICRON MOS TRANSISTORS[1]

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Using Monte Carlo simulation for examining the behaviour of submicron MOS transistors, the results are rather the properties of each individual carrier (such as position, velocity, wave vector, carrier energy, time instant of a scattering event etc.), and not the mostly averaged quantities used in the classical semiconductor physics, determined by using statistical considerations (such as carrier concentartions, mobility of carriers, current densities etc.). This paper gives a brief description of the tools which convert the results evaluated by the MicroMOS 3 dimensional semiconductor device simulation program to the theory of the classical semiconductor device theory.

1. INTRODUCTION

Assuming a silicon MOS structure with a gate area of $0.25 \times 0.25\ \mu m^2$ and a doping density of $10^{23}\ m^{-3}$, the number of ionized impurities in the depletion layer under the gate is about 10^3. The number of carriers in the inversion layer is the same order of magnitude. The relatively small number of carriers and the increasing computing power of the up-to-date supercomputers suggest the development of such a 3-dimensional Monte Carlo simulator program for studying the MOS transistor behaviour, where *the trajectories of each carrier are individually followed* both in the real space and in **k**-space (wave vector space).

Using Monte Carlo simulation for examining the behaviour of submicron MOS transistors, the results are the properties and conditions of each individual carrier (such as *carrier position, carrier velocity, carrier wavevector, carrier energy*, time instant of a *scattering event*, etc.) The quantities used in classical[2] semiconductor device thoery (such as *carrier concentrations, mobility* of carriers, *current densities* etc.) are *time- and space averages* of the quantities determined by the Monte Carlo simulation method by using various statistical considerations.

The development of a molecular dynamics Monte Carlo semiconductor device simulator represents two different kinds of tasks:

- The development of the first principle based simulator itself.
- The development of the tools to interpret the results of the Monte Carlo simulation in terms of the classical semiconductor device physics. This gives the possibility to compare the results to experimental data or to the results given by classical semiconductor device simulators. These tools can be used to apply Monte Carlo simulation results to optimal parameter determination for classical semiconductor device simulators.

Since the computer time requirement of a 3D Monte Carlo semiconductor device simulator is about 10^3 times larger than that of the classical simulators, it is very important to transfer the results as soon as possible to the models used in classical simulators.

This paper discusses the second task: how to interpret the results of the Monte Carlo simulator in terms of the classical semiconductor physics.

Tools are also required for testing the simulation results to determine whether a *maturated, stationary state* is reached or not yet.

2. PRINCIPLE OF SIMULATION

The operation of the MicroMOS 3D semiconductor device simulation program is based on the *molecular dynamics Monte Carlo method*. [1]. The channel region, together with a limited part of the source, drain and neutral bulk regions is simulated by the Monte Carlo method. On the boundaries of the last three regions charge neutrality is forced. Other parts of the device, outside of these regions, are taken into consideration by boundary conditions arising from the classical semiconductor device theory [2], [3]. Fig. 1 shows the simulated structure.

For describing the carrier — band structure interaction (i.e. the dispersion relation of carriers) the *effective mass* concept is used.

The realistic description of the *carrier dynamics* is the most important question for a Monte Carlo simulation. The concepts used in MicroMOS are the followings:

- In the *real space* the carrier dynamics is descirbed by *field – carrier interactions* based on the *Newtonian laws*. In Newton's laws only the electrostatic forces are taken into consideration. Forces arising from the magnetic

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[2] In the following the terms of classical semiconductor device theory or classical semiconductor device simulators are used in that sense, that they are based on the *Boltzmann transport equation* or on equations derived from the Boltzmann transport equation (drift – diffusion equations or hydrodynamic semiconductor equations

field have been neglacted (although this is a usual assumption in semiconductor physics, its application is not obvious for carrier — carrier interactions in low field regions). For electrons, an anisotropic effective mass tensor is used assuming six ellipsoidal constant energy surfaces in the k-space (wave vector space). Fig. 2. shows the six constant energy ellipsoids of electrons in the k-space.

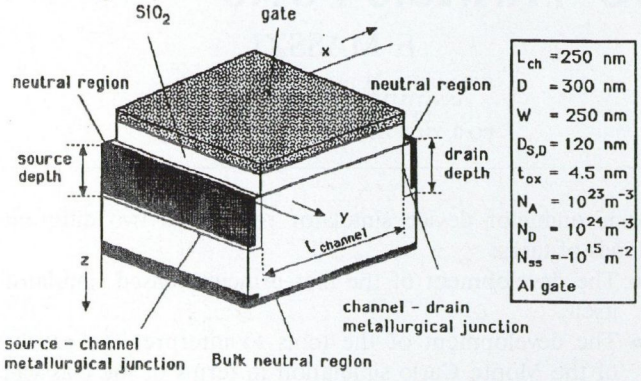


Fig. 1. The simulated structure. The active region is simulated by molecular dynamics Monte Carlo method. The active region is the channel region, and limited volumes of the source, drain and bulk neutral regions. Outside the active region classical approximations are used.

The two warped hole energy surfaces (heavy and light holes) are approximated by two spherical constant energy surfaces yielding two different scalar effective masses. The split-off holes are not taken into consideration.

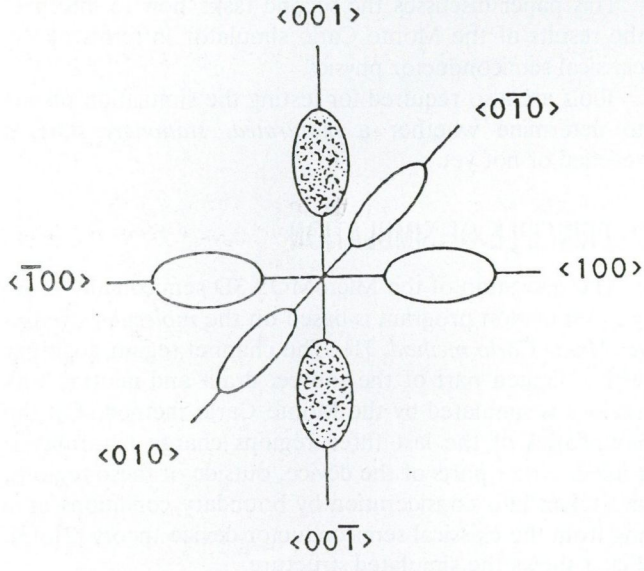


Fig. 2. Constant energy surfaces of electrons in the k-space

- In the *momentum space* (i.e. the wave-vector space) the carrier dynamics is characterized by the *carrier — phonon (lattice vibration) interactions*. In the present version of the simulation progaram a simple principle, based on thermodynamics, has been used for describing the intervalley scatterings (each electron corresponds to that ellipsoid, in which it has minimal energy). In a next version of the MicroMOS progaram a real phonon dispersion reltion will be used to describe the carrier — phonon interactions.

At present, in the MicroMOS simulation program the *surface quantization* is not taken into considearation. These effects will be included in the next versions.

3. COMPARISON OF THE RESULTS OF CALSSICAL SEMICONDUCTOR DEVICE SIMULATION AND MONTE CARLO SIMULATION

As mentioned in the introduction, the classical semiconductor device simulators, based on the *drift — diffusion equations* or on the *hydrodynamic semiconductor equations* and the *molecular dynamics Monte Carlo method* results in different kinds of physical quantities.

We focus our attention only to the d.c. simulation because the computing speed of today's supercomputers is still too slow for transient simulations. If we speek about transient conditions, this is used in the sense, that the Monte Carlo simulation has not yet reached a maturated, stationary state.

Important, to note, that for a short time interval, the circumstances are chaotic in the system, for the quantities used in the classical semiconductor physics. Only a time average (for a time period long enough) can give an acceptable result for the concentration distributions, current densities or currents etc.

3.1. Quantities determined by classical semiconductor device simulators

The solution algorithms of the classical semiconductor device simulators use only three variables for the d.c. simulation. During the simulation, these are determined for each elementary volume. These variables usually are

- the *electron concentration* $n(x_i, y_i, z_i)$,
- the *hole concentration* $p(x_i, y_i, z_i)$,
- the *potential* (e.g. electrostatic potential) $\psi(xi, yi, zi)$.

Other sets of variables can be used, but applying the methods of basic semiconductor physics, these can easily be converted into the above mentioned variables.

During the simulation various secondary quantities are also obtained, such as

- *electron mobilities* $\mu_n(x_i, y_i, z_i)$,
- *hole mobilities* $\mu_p(x_i, y_i, z_i)$,
- *generation — recombination rates* of the carriers
- *electron quasi-Fermi levels* $\Phi_n(x_i, y_i, z_i)$,
- *hole quasi-Fermi levels* $\Phi_p(x_i, y_i, z_i)$,
- *electron current densities* $j_n(x_i, y_i, z_i)$,
- *hole current densities* $j_p(x_i, y_i, z_i)$,
- the components of the *electric field vector* $\mathbf{E}(x_i, y_i, z_i)$, given by the negative gradient of the electrostatic potential,
- *electron currents of the electrodes*, given by the integrals of electron current densities perpendicular to the surface of the given electrode,
- *hole currents of the electrodes*, given by the integrals of hole current densities perpendicualr to the surface of the given electrode,
- etc.

3.2. Quantities determined by the Monte Carlo simulation

The Monte Carlo simulation program gives the following results for each simulation time instant:

- The *position coordinetes* of each individual carrier. Fig. 3 shows the carrier distribution in the simulated structure;
- The *velocity vector (or wave vector)* components of each individual carrier;
- The **k**-space coordinates and the *ellipsoid* or *sphere*, to which the carrier corresponds at the given simulation time instant;
- A list of scattering events;
- A list of carriers entering/leaving the structure;
- The *potentional* (in case of the MicroMOS simulation program, the potential components arising from dopant ions, electrons, holes, charged interface states and from external voltages) on a 3 dimensional grid. All potentional components are separately known.

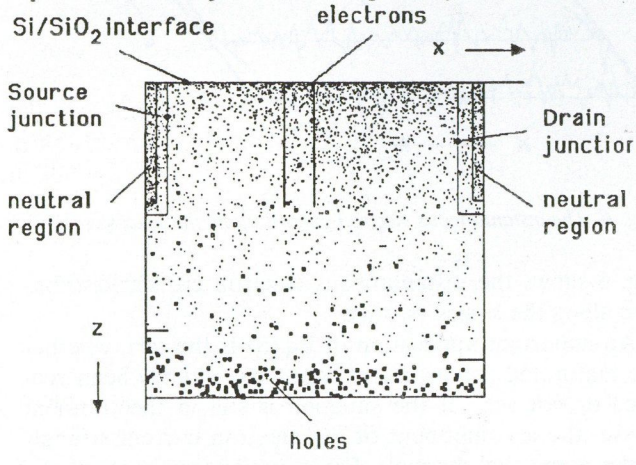


Fig. 3. Electron and hole distribution in the simulated structure

4. INTERPRETATION OF MONTE CARLO SIMULATION RESULTS IN TERMS OF CLASSICAL SEMICONDUCTOR DEVICE PHYSICS

Since the Monte Carlo simulation program gives the dynamics and of the behaviour of each individual carrier, while classical semiconductor device simulation methods use the terms of classical semiconductor device theory — based on some statistical considerations — it is necessary to interpret the Monte Carlo simulation results in terms of classical semiconductor device theory.

The *carrier concentrations* are defined as the time average of the number of carriers in a unit volume. Let $N(x,y,z,t)$ be the number of carriers (electrons or holes) in an elementary volume at the position coordinates x, y, z

$$\Delta V(x,y,z) = \Delta x \cdot \Delta y \cdot \Delta z \tag{1}$$

and at the time instant t.

The concentration of electrons or holes is given by

$$n,p = \frac{\frac{1}{T}\int_0^T N(x,y,z,t)dt}{\Delta V(x,y,z)} \tag{2}$$

The time interval T should be large enough to reach a stationary (maturated) state. The required time interval T can be determinated by a regression analysis of $N(x,y,z,t)$. If the average is stationary (i.e. the slope of the regression line for a time interval T is zero or small enough), T can be accepted, ohterwise more simulation steps are necessary. Fig. 4 shows the instantenous distribution of the electron concentration along the x-axis vs. time.

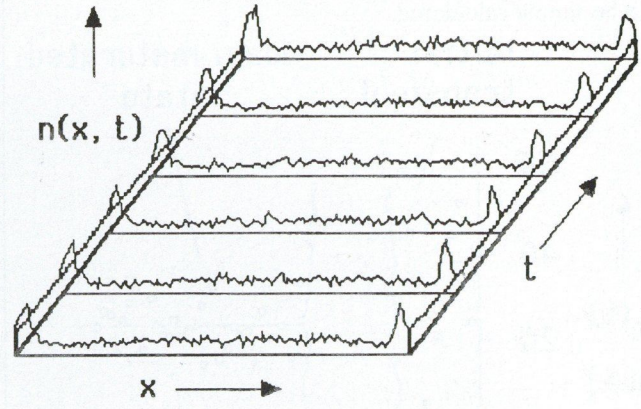


Fig. 4. The instantenous concentration along the x-axis vs. time

The *scattering rates* can be evaluated by using the number of scattering events observed during one simulation step, divided by the time increment Δt between the simulation steps. If N_i i-type scatterings happened, the scattering rate for the i-type scattering is given by

$$S_i = \frac{N_i}{\Delta t} \tag{3}$$

The *mobility of carriers* is related to the scattering rates as

$$\mu = \frac{q}{m}\sum_i \frac{1}{s_i} \tag{4}$$

In Eq.(4) it is assumed that the scattering rates s_i for the various types of scattering are independent from each other (i.e. the Mathiessen's rule is applied).

The study of the weight and importance of the various scattering mechanisms gives possibility to optimal parameter extraction mobility models for classical semiconductor device simulation programs.

The *current density* is given by the charge flux on a unit surface. The charge flux can be determined by counting those carriers, which are entering into, or leaving from the examined elementary volume during the simulation step. By counting these particles, each carrier moving in the positive direction increments the number of carriers crossing the examined surface (N) by one, while a carrier moving in the negative direction decrements it by one. For example, for an elementary surface ΔA being perpendicular to the x-direction, the x-component of the current density is given by

$$j_x(x,y,z,t) = \pm\frac{q \cdot N}{\Delta t \cdot \Delta A} \tag{5}$$

The $+$ sign is valid for the hole current density, while the $-$ sign for the electron current density.

This concept can also be applied to calculate the drain current, by counting the electrons passing through the channel-drain metallurgical junction.

Fig. 5 shows the drain current arising from the electrons passing through the channel-drain metallurgical junction, averaged for 0.3 ps. Caused by the heuristic approach of the initial carrier distribution a large inital transient can be shown. The fluctuation is also quite large in the maturated state. From the fluctuation the noise current of the device can be simply calculated.

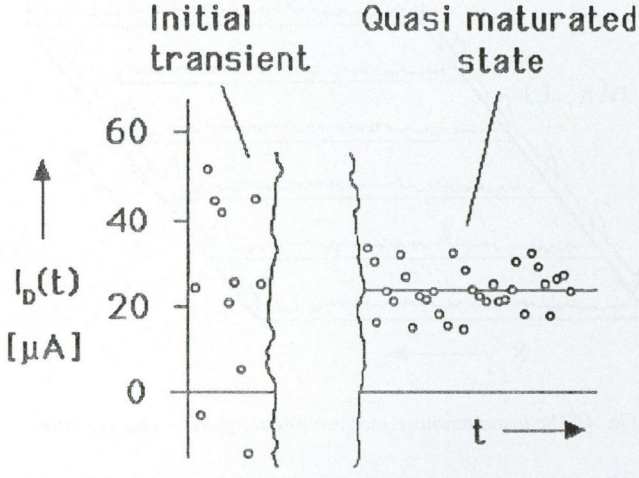


Fig. 5. The instantenous drain current vs. time

It is possible to distinguish between current densities transported by carriers corresponding to various ellipsoids (in case of electrons) and current densities transproted by light and heavy holes.

Another possibility for determining the current (or current density) is based on known carrier velocities. The current can be determined by summarizing all electron or hole velocities (for example their x components) at x in each sheet having a thickness Δx, and an area perpendicular to the x direction $D \cdot W$. Let the sum of the velocities in a sheet be Σv_x. Then the current is given by

$$i_x(x,t) = \pm \frac{q \cdot \Sigma v_x}{\Delta x} \qquad (6)$$

The $+$ sign is valid for hole current, while the $-$ sign for electron current. The sum is carried out for the velocities all of those electrons, for which the x coordinate value is in the interval of

$$x_i \leq x \leq x_i + \Delta x$$

Here it is also possible to distinguish between the current transported by the carriers corresponding to various ellipsoids (in case of electrons) and the current transported by the light and the heavy holes.

The time averages are given as follows:

- for the x component of the current density the time average is given by averaging the instantaneous values given by Eq.(5)

$$\bar{j}_x(x,y,z) = \frac{1}{T}\int_0^T j_x(x,y,z,t)dt \qquad (7)$$

- for the current flowing in the x direction the time average is given by averaging the instantaneous values given by Eq.(6)

$$\bar{i}_x(x) = \frac{1}{T}\int_0^T i_x(x,t)dt \qquad (8)$$

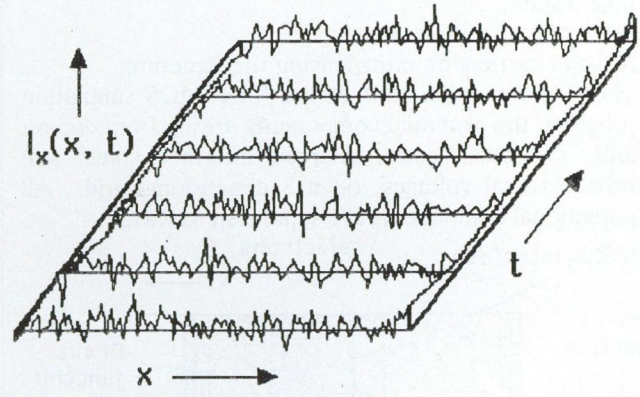


Fig. 6. The instantaneous electron current along the x-axis vs. time

Fig. 6 shows the instantaneous electron current distribution along the x-axis vs. time

An important application of Eq.(8) is the test, whether the maturated (nontransient) state has already been reached or not yet. If the situation is still in the transient phase, the x-component of the electron current strongly varies along the channel. For a stationary situation, the time average of the current must satisfy the Kirchhoff law of current contnuity: for all x-coordinates, the time average of the current's x component should be equal. By evaluating the distribution function of the current along the x-axis, information can be obtained whether the simulation is still in the transient state or it is already maturated. For a maturated situation, the distribution function is a step function.

It is relatively easy to evaluate the various potential components in the sturcture, because their values can be easily, calculated on a 3D grid. This is similar to the classical simulation methods. The only difference is, that in our case all components (the potential arising from dopant ions, electrons, holes, charged Si/SiO_2 interface states and the potentials arising from the external voltages) are independently known.

Fig. 7 shows the potential components.

- arising from the *charges in the active region* (dopant ions, charged interface states, electrons and holes);
- arising form the *external voltages* (i.e. from boundary conditions), and
- the *resulting potential distribution*

As expected, the potential distributions are not so smooth, as given by the classical semiconductor device simulator. Smooth distributions can be reached by time averaging the results over a larger number of simulation steps.

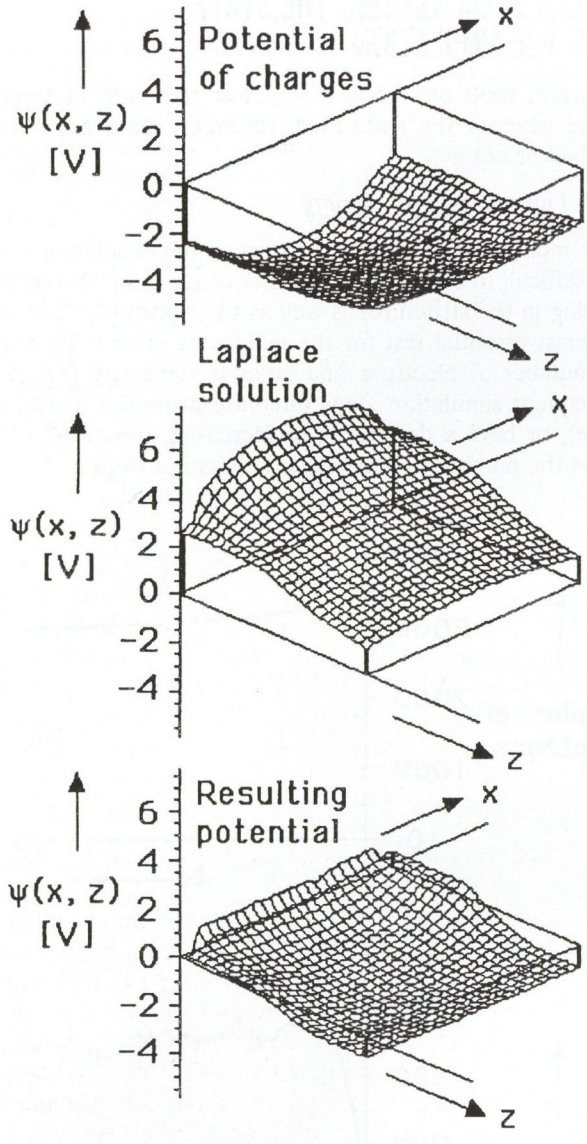


Fig. 7. The instantaneous potential distribution
a) component arising from charges in the acitve region;
b) component arising from external voltages (i.e. the solution of the Laplace equation);
c) the resulting potential distribution.

5. SPECIAL RESULTS OF THE MONTE CARLO SIMULATION

The Monte Carlo simulation method also gives some results being not directly used the classical semiconductor device theory. However, these results represents, important aspects for the understanding of the processes playing an important role in the operation of the semiconductor device.

5.1. Velocity distribution

An interesting result of the Monte Carlo simulation is, that it determines the velocity distribution of the carriers in the simulated structure as well. Fig. 8 shows the electron velocity distribution in the velocity space for the electrons corresponding to each ellipsoids, and the resulting velocity distribution, seen from the y-direction

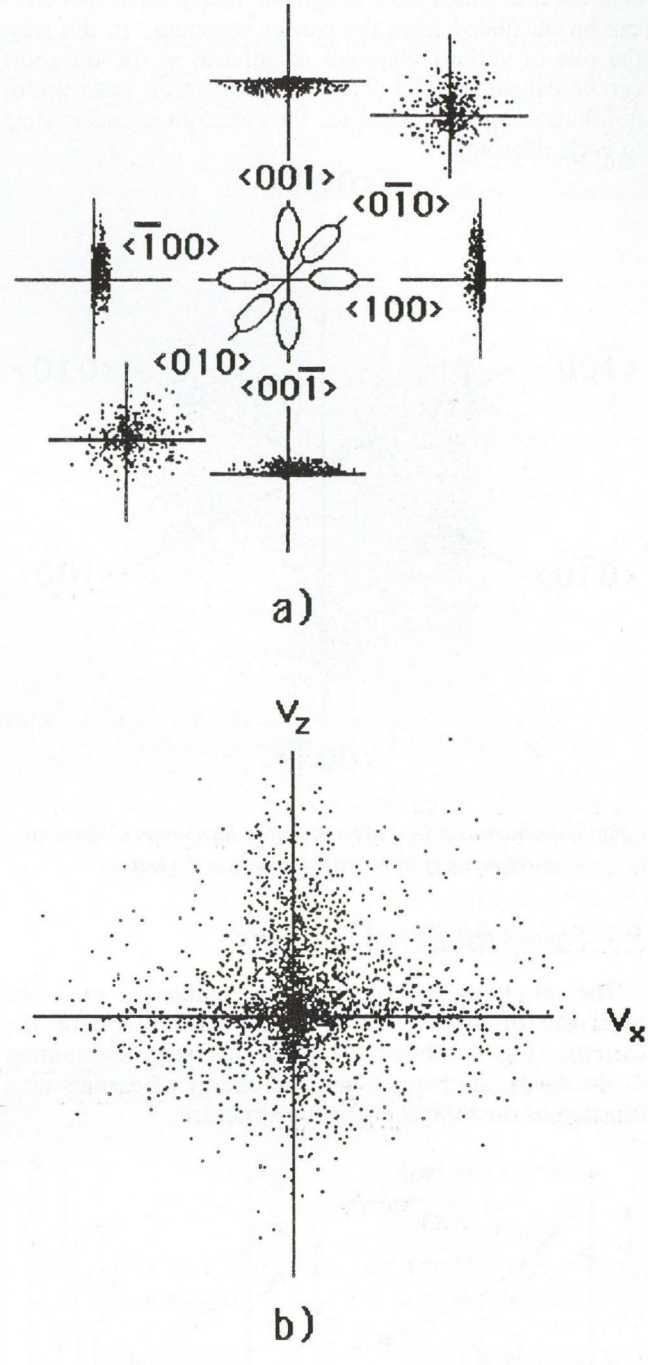


Fig. 8. The velocity distribution of electrons in the velocity space (as seen from the direction of the y-axis)
a) the components corresponding to various ellipsoids;
b)the resulting velocity distribution.

The figure shows that the first momentum (the center of wieght) of the velocity for the electrons corresponding to the $< 0\bar{1}0 >$, $< 00\bar{1} >$, $< 010 >$ and $< \bar{1}00 >$ valleys is shifted in the positive x direction. These electrons contribute signifiantly to the current, as expected from theory.

5.2. k-space (wave vector) distribution

Since it is known, which electron corresponds to which ellipsoid and which hole is light or heavy, their **k**-vectors can be calculated from the carrier velocities. In this way, the role of various ellipsoids or spheres in the transport can be examined. Fig. 9 shows the electron wave vector distribution in the **k**-space for the electrons corresponding to each ellipsoids.

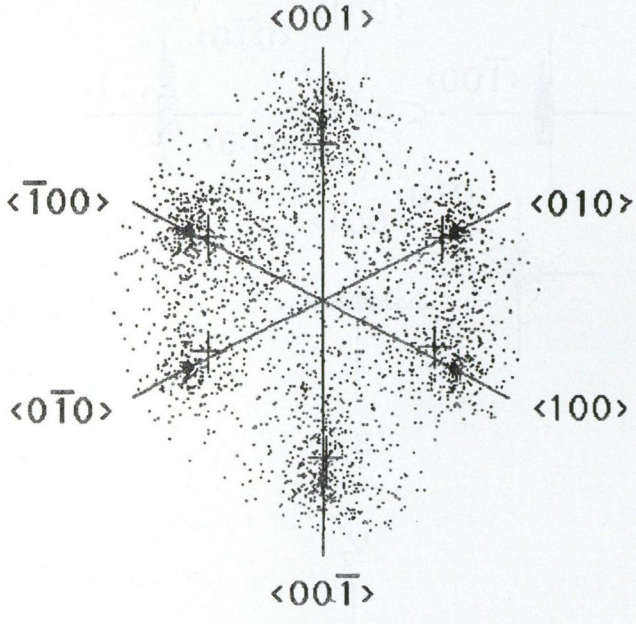


Fig. 9. Axonometric view of the **k***-vector distribution of electrons corresponding to various ellipsoids in the* **k***-space*

5.3. Energy distribution of carriers

The results of the Monte Carlo simulation gives the possibility to determine the energy distribution of the carriers. Fig. 10 shows the electron energy distribution in the inversion channel, and the energy of carriers as a function of the time spent in the structure.

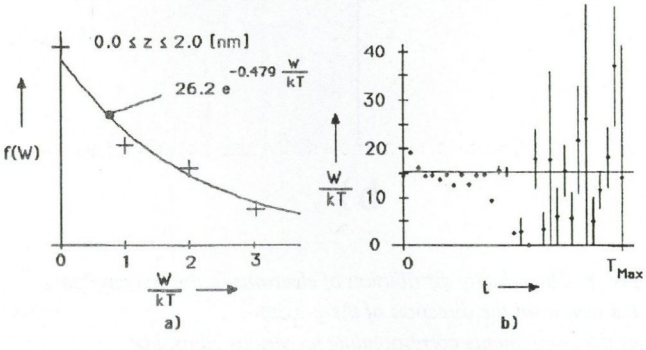


Fig. 10. The energy distribution of electrons
a) the distribution function near the Si-SiO_2 interface;
b) the energy distribution vs. the time spent in the structure. The vertical bars show the influence of ± 1 electron.

It is interesting to observe the exponential distribution of the electron energies, proving that the simulation results satisfies the Maxwell–Boltzmann distribution law (which is never used during the simulation).

6. TOOLS FOR TESTING THE STATE OF THE SIMULATION

Several tools are necessary to test the state of simulation, whether the maturated, stationary state has been reached or not get.

6.1. The number of carriers

As mentioned earlier, at the start of the simulation it is very difficult to estimate the number of electrons and holes residing in the structure, as well as their position. One of the most essential test for the maturated state is [4] that the number of electrons and holes is stationary (i.e. in subsequent simulation steps fluctuate around a constant value), or have a decreasing or increasing trend. Fig. 11 shows the number of carriers vs. simulation steps.

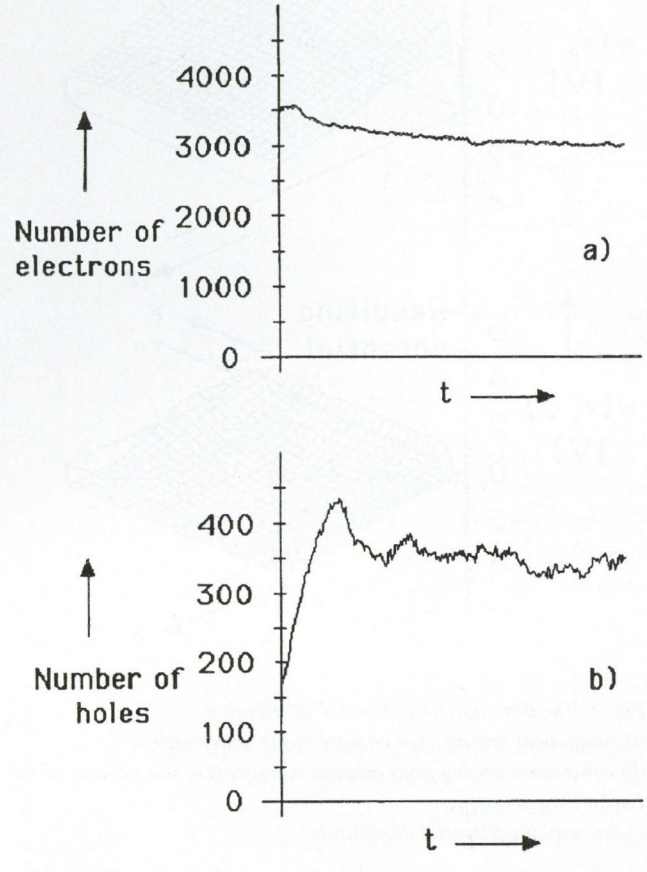


Fig. 11. The number of carriers vs. time
a) electrons;
b) holes.

6.2. The age distribution of carriers

Since at the start of the simulation a heuristic initial carrier distribution is injected into the structure, it is a realistic assumption, that the maturated situation can be reached only after these initial carriers depart the channel region. For testing the simulation state, the density function and distribution function can be applied. The *normalized discrete density function (spectrum)* for a variable y at the i-th x interval is given as

$$f(x_i) = \frac{y(x_i \le x \le x_i + \Delta x)}{\sum_i y_i} \qquad (9)$$

and the *distribution function (cumulated distribution function)*

$$P(x_i) = \sum_{j=1}^{i} f(x_j) \qquad (10)$$

Evaluating density and distribution functions for the time spent in the structure, we get some information about the simulation state. Fig. 12 shows the time average for the time spent in the structure (spatial distribution, density and distribution functions).

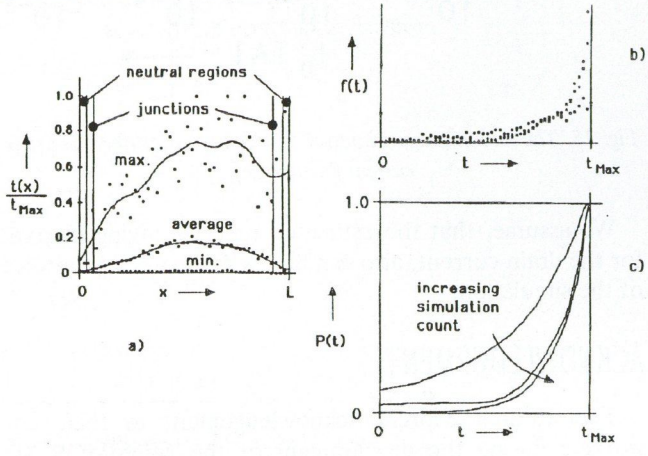
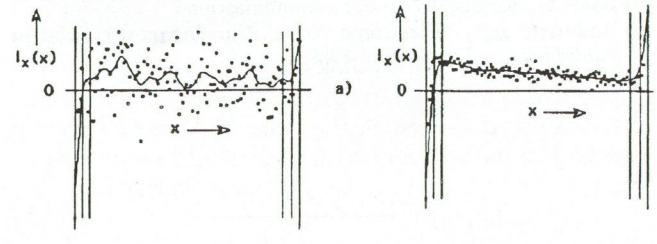


Fig. 12. The time spent in the sturcture at various stages of the simulation (electrons)
a) averaged spatial distribution;
b) density function;
c) distribution function.

6.3. The current distribution function

An imported information can be obtained from the density and distribution functions of the time average of the current flowing along the channel (i.e. x direction), calculated according the Eq.(6). In an ideal case (assuming that the gate, bulk and displacement currents are negligibile), the *Kirchhoff's current conservation law* must be satisfied, i.e. it should be a constant current for each x position. For this case the density function is a *Dirac – delta function* and the distribution function is a *step – function*. The spatial distribution of the time average, together with the density and distribution of the time average, together with the denstiy and distribution functions for the x-component of the electron current are shown Fig. 13.



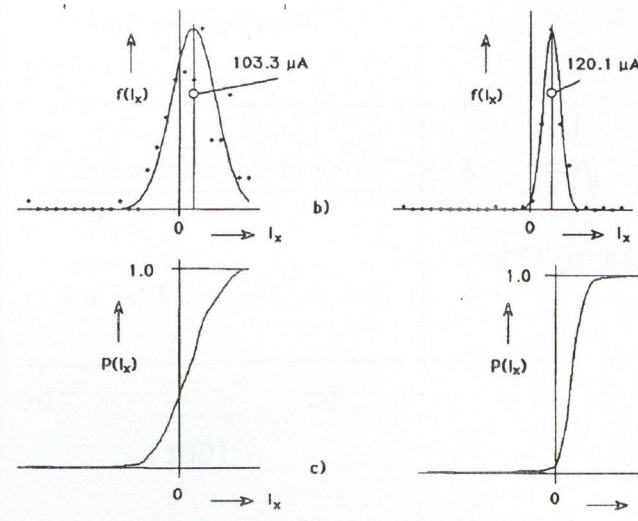


Fig. 13. The conduction current along the x-axis
a) averaged spatial distribution;
b) density function;
c) distribution function.
For a maturated condition the time average of the density functions should be a Dirac – delta function *and the time average of the distribution function is a* step function. *It is assumed that the displacement current can be neglacted.*

The figure shows one instantaneous and the time averaged distributions.

6.4. The shot-noise as a quantity for estimation averaging time interval

In order to get an estimation for the required averaging time interval for the current, calculated from the electrons passing through the channel – drain junction, the following method can be used:

The *Schottky theorem for electronic noise* [5] gives for the drain current *rms shot-noise* the

$$\overline{i_D^2} = 2qI_D\Delta f \qquad (11)$$

value. The drain current rms shot noise for a bandwidth of $\Delta f = 1/\Delta\tau$ is given by

$$\frac{\sqrt{\overline{i_D^2}}}{I_D} = \sqrt{2}\sqrt{\frac{q}{I_D\Delta\tau}} \qquad (12)$$

The noise, given by the simulation, can be calculated by linear regression of the function of electrons passing through the channel-drain junction vs. time. Fig. 14 compares the theoretical and simulated rms noise drain currents, related to unit bandwidth, as a function of frequency. As excepted, the drain current rms noise is a little higher, as the pure shot-noise (according our experiences, about $\alpha = 1.5$ times higher).

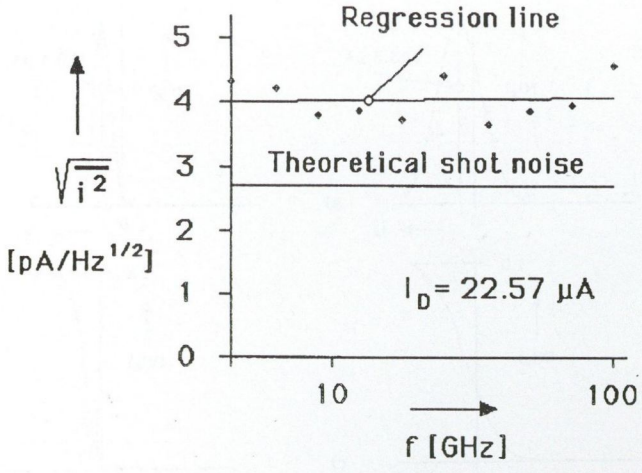


Fig. 14. Shot noise of the drain current

In this way for the estimation of the required time averaging interval a theory based criteria can be given. The required time averaging interval (using the Eq. 12 with an enhancement factro α) is given by

$$\Delta\tau = \frac{2\alpha^2 \frac{q}{I_D}}{\left(\frac{\overline{i_D^2}}{I_D^2}\right)} \qquad (13)$$

Based on Eq. 13, Fig. 15 shows the time averaging interval vs. current for a drain current uncedrtainty of 5% (with $\alpha = 1.5$). As seen from the figure, if the current is less than 10 μA, the duration of the required time averaging interval $\Delta\tau$ grows over 20 ps. Since the elementary time step dt of simulation — in order to follow the real carrier trajectories, — must be less, then 0.02 ps, this requires more than 1000 simulation steps and results in an extremely long CPU time (for Alpha chip Series 5000 DEC work stations over 400 hours). Important to note, that in case of lower currents, the number of electrons is smaller. Since the time requirement of a simulation step depends quadratically from the number of point charges in the structure, the time of simulation steps decreases. Therefore the above simulation time increment is overestimated.

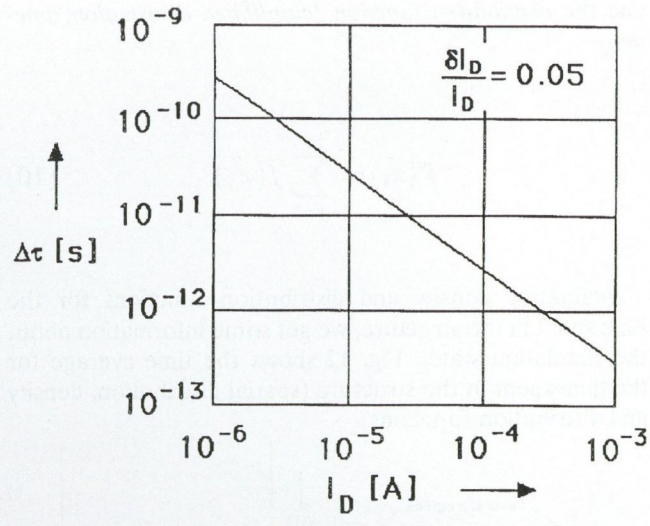


Fig. 15. The time averaging interval vs. drain current (for 5% drain current fluctuation)

We assume, that the estimated time averaging interval for the drain current, also can be used for other quantities of the simulation.

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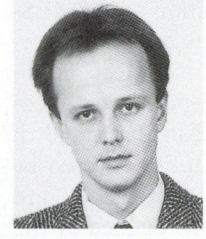

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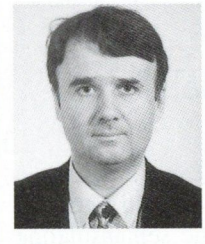

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MODELLING ELECTRO-OPTICAL INTERACTION IN MESFETS

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A modelling procedure is presented for MESFETs with both electrical and optical inputs. First a physical model is introduced for the illuminated MESFET. The actual circuit model with electrical and optical variables is developed from measured S-parameters of the device by calculating a set of linear circuit models and by approximating the linear circuit elements with two-variable nonlinear functions.

1. INTRODUCTION

Several models have been developed for microwave MESFETs with large electrical inputs [1-2]. However, for simultaneous electrical and optical excitations [3-4] general MESFET models are not available presently.

In this contribution a modelling procedure is outlined for representing the high-frequency operation of the MESFET with both electrical and optical inputs. The procedure starts with presenting the physical model of illuminated MESFETs. That is followed by S-parameter measurements in a wide frequency band and in the range of electrical and optical variables, that are to be covered by the model. Secondly, a set of linear circuit models are developed for the different operation points defined by the electrical and optical variables. At last the set of various circuit element values are approximated by two variable nonlinear functions using curve fitting procedures. The resulting circuit model is suitable for analyzing MESFETs with large electrical and optical inputs.

2. THE PHYSICAL MODEL OF ILLUMINATED MESFETS

The operation of a MESFET device can be described by a simple electrostatic physical model. The structure of the device is presented in Fig. 1. On the semiinsulating substrate a semiconducting epitaxial layer is grown. The drain (D) and source (S) electrodes have ohmic contacts to the epitaxial layer. However, at the gate (G) a metal-semmiconductor junction is established and because of its potential barrier a depletion layer is created below the gate

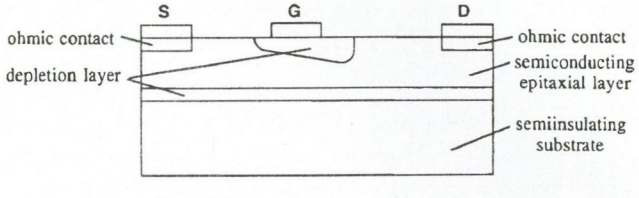

Fig. 1. The structure of the MESFET device

as shown in Fig. 1. A potential difference exists between the substrate and the epitaxial layer also therefore a depletion layer is created between them as well.

In the depletion layers there are no charge carriers thus they behave like insulators. The conductivity of the semiconducting epitaxial layer is high enough, thus it serves like a conductor, and therefore the depletion layers can be considered as capacitors in the equivalent circuit of the device. Fig. 4 shows the equivalent circuit of the MESFET where C_g represents the capacitance between the gate and source, C_d is the capacitance between the drain and source, and C_r is the capacitance between the drain and gate providing a feedback from the output to the input. Nevertheless, the resistance of the epitaxial layer is not completely negligible, thus reistors appear in the equivalent circuit between the gate and source (R_1) as well as between the drain and source (G_d).

The basic operation of the MESFET is determined by the voltage dependence of the depletion layer next to the gate area, resulting in the variation of the junction capacitance and the drain current.

The effect of illumination is dependent on the optical absorption in the device material. If the optical absorption coefficient is too high most of the photons will be absorbed at the surface and their effect on the device performance will not be significant. On the contrary if the optical absorption coefficient is too small only a part of the photons will be absorbed inside the device and their effect will again not be significant. The absorption coefficient is dependent on the optical wavelength therefore the wavelength of the illuminating light should be chosen properly.

The absorbed photons generate charge carriers which carriers reduce the potential barrier. This effect is called the photo-voltaic effect. According to the theory [4] and experiments [5] the photo-voltage is a logarithmic function of the absorbed light intensity.

Applying the appropriate illumination the light is absorbed in the vicinity of the depletion layers. Thus charge carriers will be generated in both depletion layers reducing their thickness. Charge carriers will also be generated in the epitaxial layer and in the substrate increasing the conductivity. The increased conductivity of the epitaxial layer makes no significant change because the conductivity of this layer is high enough in the dark case as well. However, there is a remarkable change in the substrate due to the illumination because the originally semiinsulating material becomes semmiconducting and thus current can flow in the substrate, too.

The illumination makes changes in the elements of the equivalent circuit based on the beforegoing physical effects. As the thickness of the depletion layer is decreased the capacitances and the drain-source current are increased. The latter is enhanced due to another effect as well, namely the originally insulating substrate becomes conductive due to the photon absorption, and thus current will flow through it between the drain and source.

Consequently, all elements of the equivalent circuit describing the inner part of the device are dependent on the illumination. This dependence will be investigated based on measurements of the scattering parameters carried out in a wide frequency range at several biasing voltages.

3. S-PARAMETER MEASUREMENTS

In the followings we investigate the HP MESFET type HFET 1101. The S-parameter measurements were carried out by using the HP Network Analyzer type HP 8409/A. Optical illumination was provided by a laser equipment with 780 nm wavelength.

Representative S_{21} parameters are shown in Fig. 2 in the frequency range $2 - 10$ GHz for the operating point $U_G = -1,5$ V, $U_D = 4$ V with 0 μW and 600 μW illuminating powers. In the illuminated case an approximately 2 dB increase was obtained in the S_{21} parameter, which decreased at higher frequencies. Considerable changes were observed in the reflection parameters S_{11} and S_{22} also.

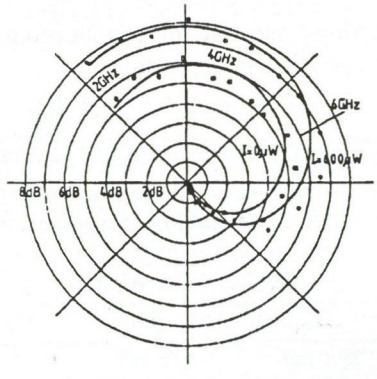

Fig. 2. S_{21} parameters

To develop a two variable circuit model for the MESFET in the gate voltage range $U_G = (-2$ V, 0 V) and the optical power range (0 μW, 600 μW) S-parameters of the device have been measured at 10 different value-pairs of the electrical and optical variables as illustrated in Fig. 3. Using the measured S-parameter values linear circuit models, comprising 14 circuit elements have been determined in all 10 operating points by a circuit optimization program.

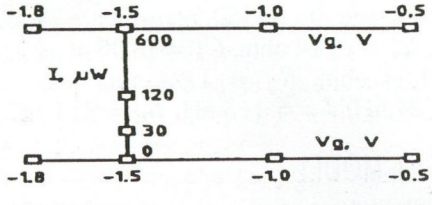

Fig. 3. Operating points for modelling measurements

4. EQUIVALENT CIRCUIT

The circuit model for the MESFET is given in Fig. 4. The measured S-parameters have been approximated by a modelling routine. From several runs of this program it has been observed that the set of S-parameters can be represented accurately with a circuit model having 4 elements depending on the operating point variables and 10 elements being independent of the electro-optical variables. The variation of the gate voltage and the optical intensity produced considerable changes in the circuit elements G_m, G_g, G_d, C_g. On the other hand the parameters R_g, L_g, R_s, L_s, R_d, L_d, C_d, T, R_1, C_r have not been changed significantly.

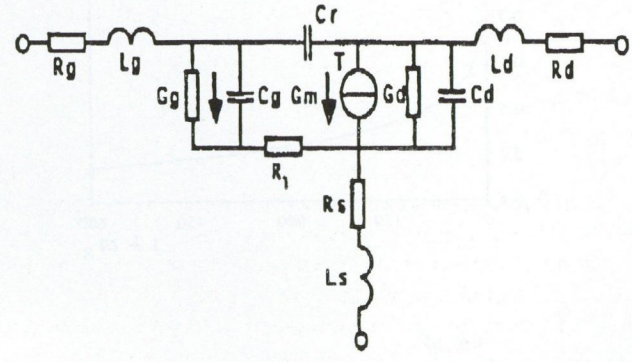

Fig. 4. MESFET equivalent circuit

The optical intensity dependence was approximated at the gate voltage $U_G = -1,5$ V. The measured values are given in Table 1.

Table 1. Intensity dependence at $U_G = -1.5$ V

I, μW	0	30	120	600
G_m, mS	18,7	24,0	25,1	27,4
G_g, mS	0,79	0,57	0,48	0,37
G_d, mS	0,77	1,98	2,46	3,08
C_g, pF	0,47	0,48	0,484	0,49

The admittance-intensity characteristics are shown in Fig. 5. It was found that a logarithmic curve could be fitted to the measured points in the form:

$$Y = A + B \lg(1 + I/I_R)$$

with the reference power $I_R = 1$ μW the coefficients A and B are summarized in Table 2.

Table 2. A and B parameters at $U_G = -1.5$ V

	G_m, mS	G_g, mS	G_d, mS	C_g, pF
A	18,7	0,79	0,77	0,47
B	3,13	−0,15	0,83	0,007

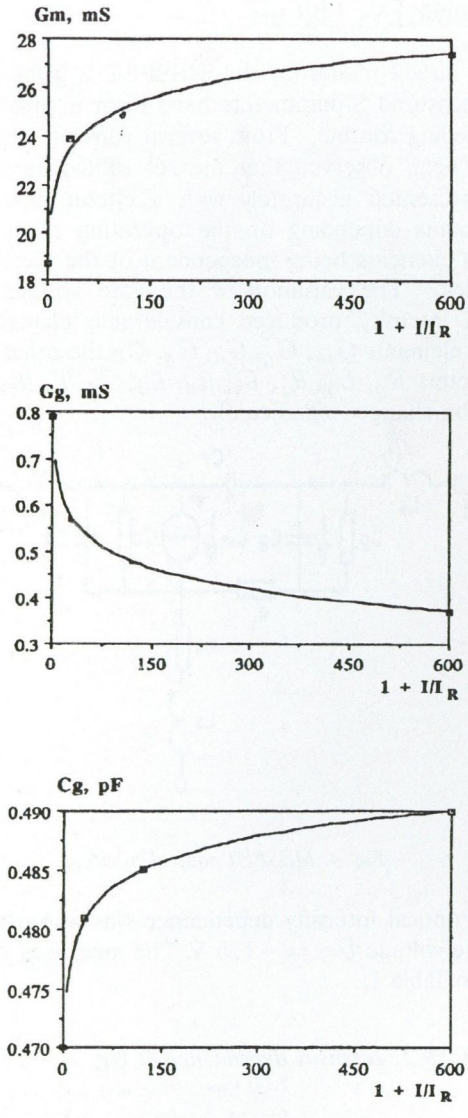

Fig. 5. Admittances vs. optical power

Next the gate voltage dependence of the measured parameters was approximated. The measurements have shown gate voltage dependence of the input and the transfer admittances. The voltage dependent circuit element values for $I = 0$ μW and $I = 600$ μW are given in Table 3 and Table 4, respectively.

Table 3. Gate voltage dependence with $I = 0$ μW

U_G, V	−1,8	−1,5	−1,0	−0,5
G_m, mS	12,9	18,7	23,3	27,8
G_g, mS	0,65	0,79	0,88	1,0
C_g, pF	0,42	0,47	0,51	0,56

Table 4. Gate voltage dependence with $I = 600$ μW

U_G, V	−1,8	−1,5	−1,0	−0,5
G_m, mS	23,5	27,4	29,6	30,2
G_g, mS	0,14	0,37	0,58	0,72
C_g, pF	0,44	0,49	0,53	0,59

The admittance-voltage characteristics are shown in Fig. 6.

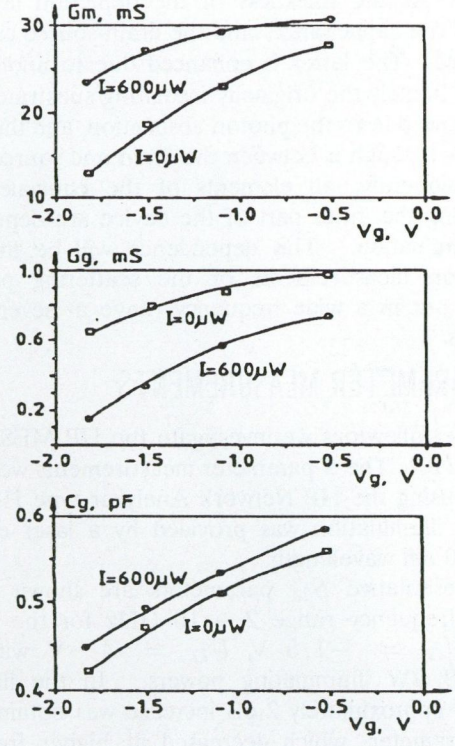

Fig. 6. Admittances vs. gate voltage

The following functional form produced a good approximation for the element characteristics:

$$Y = [A_1 + A_2 U_G + A_3 U_G^2] + \\ + [B_1 + B_2 U_G + B_3 U_G^2] \, lg \, [1 + I/I_R] \qquad (1)$$

The A and B coefficients of the nonlinear characteristics are given in Table 5 and Table 6, respectively.

Table 5. A coefficients

	G_m, mS	G_g, mS	C_g, pF
A_1	29,1 mS	1,05 mS	0,59 pF
A_2	0,75 mSV^{-1}	0,065 mSV^{-1}	0,05 pFV^{-1}
A_3	−4,47 mSV^{-2}	−0,082 mSV^{-2}	0,02 pFV^{-2}

Table 6. B coefficients

	G_m, mS	G_g, mS	C_g, pF
B_1	−0,64 mS	−0,12 mS	0,014 pF
B_2	−3,31 mSV^{-1}	−0,064 mSV^{-1}	0,013 pFV^{-1}
B_3	−0,48 mSV^{-2}	−0,057 mSV^{-2}	0,0036 pFV^{-2}

The circuit elements found to be independent of the gate voltage and the optical intensity are as follows: $T = 14,5$ ps, $R_i = 0,14$ ohm, $C_r = 0,05$ pF, $C_d = 0,18$ pF, $R_s = 0,11$ ohm, $R_g = 1,24$ ohm, $R_d = 0,8$ ohm, $L_s = 0,24$ nH, $L_g = 1,3$ nH, $L_d = 1,1$ nH.

5. MESFET MODEL

The high-frequency operation of the MESFET has been represented by the conventional circuit topology where

some of the equivalent circuit elements are given by two variable functions as in Eq. (1). The remaining circuit elements are considered as independent of the operating point variables. The model is suitable for performing analysis of circuits comprising the MESFET device with optical illumination.

6. ILLUSTRATIVE EXAMPLE

We use the MESFET model for calculating the gain and distortion of an amplifier stage with HFET 1101. The gain of a tuned MESFET stage operating between source and load impedances $R_S = R_L = 50$ ohm is given by:

$$A = \frac{R_L G_m(U_G, I)}{[1 + R_S G_g(U_G, I)][1 + R_L G_d(U_G, I)]} \quad (2)$$

The third order distortion measure D_3 can be expressed by the admittance function coefficients. For a polynomial admittance function:

$$G_i = G_{i1} + G_{i2} U_G + G_{i3} U_G^2 \quad (3)$$

$$i = m, g, d$$

the n-th order distortion measure can be expressed as follows:

$$D_n = K \frac{G_{in}}{G_{i1}^n} \quad (4)$$

where the constant K is determined by the distortion order and the reference power level.

The gain and distortion values calculated for different operating points are given in Table 7.

Table 7. Gain and distortion parameters

Operating point	(−1, 5 V, 0 μW)	(−1, 5 V, 600 μW)	(−1 V, 0 μW)	(−1 V, 600 μW)
Gain	−1, 6 dB	1,2 dB	0,8 dB	2,0 dB
Distortion	−42 dBm	−48 dBm	−49 dBm	−51 dBm

It can be seen that both the gain and the distortion are effected by the illumination. The effect is more pronounced for more negative gate voltages, however, in this case the gain is smaller and the distortion is somewhat larger.

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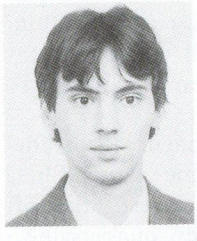

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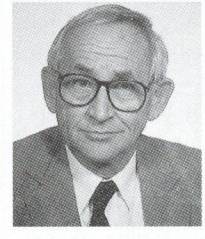

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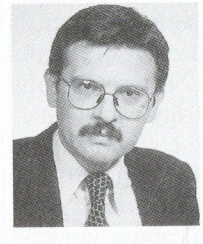

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MATERIALS RESEARCH IN HUNGARY

Any survey of a research topic usually generates bad feelings as, by Murphy'sm, there are always excellent works even groups which had been left out uninternationally. Therefore, apologies from the reviewer accompanies this survey.

In the last decades, Hungary and Poland had a special relation to the West, which allowed scientists to make use of the consent or neutrality of governments, when scientific contacts were concerned. Thus, a big number of *bona fide* researchers used the favoured position to build sincere personal relations and to do successful research at the same time.

As relations were more or less randomly organized, the now existing spectrum of research in these two countries became extremely broad, as each scientist tried to carry on his successful topic at home and to keep warm relations with his Western partner. Most Western partners were aware of the importance of these contacts and reacted correspondingly.

As for Hungary, science has flourished relatively well and has received a good acceptance in the West, because a vast majority of the valuable work was properly published. Among many topics, materials science and/or solid state physics have always received a special attention from actual governments as a key to modernization. The choice of a theme has been motivated frequently not by the real need of industry, but by the interest of scientists. Several prototypes have been developed, but only a few have appeared as commercially available products.

Thus, the advent of the renewed political-economical system has found an up-to-date research here, nevertheless with the impression that it may be oversized in comparison with the country's needs. On the contrary, the science community is conviced that besides economists, who should reshape the economy, material scientists are definitely among those, who are also needed for the renewal. At least, the visible existence of both experienced and young engineers, scientists is the only factor, which helps to attract investments into local industry. We must accept that most of the expected investors will retain the highest level research and development in their home locations. However, to run a high-tech production and the corresponding quality control and quality assurance, should establish attractive jobs also for locals.

In the field of semiconductors, there were traditionally three major centers of research. Materials science of silicon based techniques was studied that time in the Central Research Institute for Physics, where the early experience in ion implantation was excepted to broaden. It ought to arrive at a stage, where LSI circuits can be prduced on a laboratory scale. The early research activity was mostly stopped in the late seventies and a part of the group joined a government financed activity together with two industrial research institutes (Research Institute for Electronics and Research Institute for Telecommunication) and a university chair (Chair for Electronic Devices of the Technical University) to reproduce a microprocessor equivalent to Intel's 8080. The work ended succesfully in 1980 and, simultaneously, a medium-scale facility was founded (Work for Microelectronics). This company, however, ended in a full failure of management and organization within half of a decade, burying the whole topic literally under its ashes. Only few research activities survived and remained internationally accepted, like research on ion implantation, on thin films (using ion beam analysis, RBS and other surface characterization tools, like ellipsometry, UPS etc.) and on internal gettering and device modelling [1.1-24]. The level of financing, however, shrinked to the average level of basic studies. For the work to produce devices, only one laboratory exists today within KFKI Research Institute for Materials Science, though with grade 10 and 100 laboratories being capable for about 1 μm technology. Here, the work focuses on sensors and on training of students in engineering.

At the A. József University , Szeged, strong groups were on application of lasers to submicron sturcturing [2.1-4]. Surface physics there [catalysis, 3.1-3] and the Institute for Atomic Physics Technical University Budapest and Surface Physics Group of the Hungarian Acad. Sci., Budapest, and in the Res. Inst. Atomic Phys. "ATOMKI", Debrecen, are very active and successful [3.4-20].

Another large center for semiconductor research, the Research Institute for Technical Physics, has been concentrating on compound semiconductors long since. As local industries were never interested in devices of this type, the institute developed on its own track continously and reached fine successes in LEDs and lasers based on their unique liquid phase epitaxy technique. Parallel with this work, also research became internationally known there, like the work on thin films in general and contacs of II-IV semiconductors (based mostly on accumulated knowledge in electron microscopy and other surface analysis techniques) [4.1-13]. Another special point of excellence is there on electrical characterization. A small company, Semilab, grew out from there very early. This company is known by its products (DLTS, lifetime tester) on the international market.

For materials science of non-semiconducting materials, the major centers of research were four universities (Roland Eötvös and Technical University in Budapest, the University of Heavy Industry, Miskolc, and the University of Chemistry, Veszprém), the Central Research Institute for Physics (now KFKI institutes), the Research Institute for Technical Physics and three industrial research institutes (two for aluminium and one for iron based materials).

Here several directions can be mentioned: the study of magnetic materials (including crystalline garnet films and amorphous soft magnetic alloys), the investigation of rapidly solidified materials (metallic glasses, quasicrystals,

micro- and nanocrystalline metals), the works of advanced aluminium and iron alloys and on refractory metals related to local industry. Both theoretical and experimental studies of defects and modelling of processes in the crystalline state are also an outstanding topic. High melting point oxide single crystales have been grown by a modified Czochralski method (Laboratory for Crystal Physics, and Res. Inst. Matl. Sci.) for use in lasers and magnetic bubble memory devices. The understanding of the physics of magnetism (Bloch walls) and its correlation with crystalline structure in garnet films was a successful topic on fringes of a well-financed, but controversial project to produce magnetic bubble memories [5.1-54].

As Mossbauer effect was reproduced within weeks in Hungary, it is a flourishing topic to study material systems. Similar activity covers systems accessible with other nuclear techniques [6.1-6].

Up-to-date process have been introduced like crystal growth under special gravity conditions, both metallic and semiconductor, melt spinning, mechanical alloying, surface modification by ions, laser or electron beams and problems of fatique [7.1-4].

Investigations using ion beams to simulate first wall corrosion in fusion reactors, and by use of > 10 MeV/amu energy irradiation at the Dubna Laboratories (Russia), defect studies in metallic membranes and the works on the boundaries between solid state and nuclear physics should be mentioned [8.1-11].

The following literature survey of the last years will give a flavor to the reader both about quality and diversity of such research in Hungary. As most of this research is somehow connected with education, the quality of training of young scientists and engineers may also be convincing.

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REPORT ON COST TCT/MC CHAIRMEN MEETING

The COST Technical Committee "Telecommunications" (TCT) held in June in Hungary its meeting next in turn, at first in Central Europe, in an exsocialist country, which indicates the appreciation of the Hungarian activity. The Hungarian member of TCT Professor Zombory, Dean of the Faculty of Electrical Engineering at TU Budapest was the host of the Meeting. The Meeting was organized with the support of the Commission of EC, National Committee for Technological Development (OMFB), the Hungarian Telecommunication Company Limited (MATÁV) and the Antenna Hungária, Hungarian Radiocommunications Corporation. The scene of Meeting was in the building of OMFB. Invited native experts participated also at the Meeting.

The TCT is an advisory body which directs COST Telecom activity at national level, prepares and reviews propsals for new projects and keeps abreast of progress in running porjects. Decisions are taken at level of the COST Committee of Senior Officials where the representatives of the 24 COST countries follow up all COST Activities.

The TCT Meeting involved the Management Committee (MC) Chairmen Meeting also. The running of each project is the responsibility of the project MC who also decides on workplans towards the goals defined in the Memorandum of Understanding (MoU). For each individual COST project, the form of cooperation is defined in a simple international agreement called MoU which is signed by the project participants and constitutes the basic document describing the objectives and nature of the project. The chairman of MC's reported the progress results of their projects at the Meeting. Progress results from COST procects are contained in an Annual Report, a Final Report then details the overall research findigs at the termination of the project. Most COST projects aim to promote basic applied scientific and technical research and are in the nature of pre-competitive research. They fall somewhere between fundamental research and development work. However, some COST projects have resulted in the development of new products. The flexibility and openness of the COST forum has been the basis of its success where universities, telecom operators and sometimes, industrial partners have explored new ideas and proposed solutions to specific problems of common interests.

COST Telecommunications is a framework and forum for technical and scientific cooperation between twenty four European countries joining common actions in the Telecommunications field. COST was established on the initiative of the Council of the European Communities by a Ministerial Conference in November 1971 with the aims of strengthening European industrial and scientific competitiveness through cross-border collaborative research project.

The role of COST has expanded since 1989 to include support for cooperation with Central and Eastern European countries. In 1991, a Ministerial Conference in Vienna, Austria opened COST to Czechoslovakia, Hungary, Poland and Iceland. These countries have become full COST members. Later, in February, 1992. Slovenia and Croatia were also approved as members by COST Committee of Senior Officials. Institutes belonging to other European non-COST countries can also participate at institute level. THis enlarges the partnership and is a good testbed for other types of cooperation.

Cooperation between the Cost programme and other EC programmes as well as other organizations and bodies, like standardisation duplication of work and benefiting from the complementary roles of each scheme. Under COST framework, the bottom up approach helps to identify and fill research gaps from other schemes.

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WORKSHOP ON COMPUTER AIDED METHODS AND TECHNICAL MANAGEMENT IN ELECTRICAL ENGINEERING EDUCATION

A three day working was held on June 16-18, 1993, at the Faculty of Electrical Engineering and Informatics of the Technical University of Budapest, supported mainly by the TEMPUS program, and partly by the IEEE Hungarian Section and the Hungarian Telecommunications Society.

The workshop was organized in the framework of the Faculty's TEMPUS porject, which aims "To improve the efficiency of education through advanced computer sciences and by introducing technical management and marketing studies at the Faculty of Electrical Engineering and Informatics of the Technical University of Budapest". This project was initiated by 7 departments of the Faculty:
the Department of Electron Devices,
the Department of Electromagbetic Theory
the Department of Mathematics,
the Department of Measurement and Instrumentation Engineering,
the Department of Microwave Telecommunication,
the Department of Telecommunication and
the Department of Telecommunications and Telematics.

The project is headed by Prof. László Zombory, the dean of the Faculty. The western partners of this project are
the University of Karslruhe,
the University of Erlangen-Nürnberg,
the University College London,
the Institut National Polytechnic de Grenoble,
the University of Pisa,
the Technical University of Delft,
the Motorola GmbH,
the Texas Instrument Deutschland,
the Hewlett-Packard Limited Scotland,
the Digital Equipment Corporation and
the IBM European International Serivce Center
– most of them have actively contributed not only to the curriculum development and mobility program of the TEMPUS project, but also to the success of the current workshop.

We have to emphasize in advance, that however the operation of the TEMPUS project is based first of all on the work of the initiating Departments of the Faculty, the Workshop was a broader event: lectures were delivered by the members and students of other departments of

the Faculty as well, and attendees to the workshop were invited from the whole Technical University of Budapest.

The workshop was preceded by two special courses. One of them was a two day course on "ASIC design and testing with Eurochip tools", given by the Department of Electron Devices for Faculty members and PhD. students (based on the hardware and software tools and knowledge gained by a former TEMPUS project of the Department of Electron Devices), the other was a half day course with demonstration, given by the James Martin Associates of Texas Instruments about "CASE tools in Management". Texas Instruments offered a further half day course as well, this was run parallel with the regular conference events, conducted by the Texas Isntrument's educator, S. Rózsa, about FPCA design.

The opening plenary lecture of the Workshop was delivered by Professor E. Pungor, the President of the National Committee for Technological development. He gave a very interseting presentation about the "Innovation policy of the Hungarian Government", which was followed by such a vivid discussion, that Prof. Pungor, could hardly leave the spot.

In the mornings tutorial seesions were held, mainly by the representatives of our western partners. It is difficult to choose only some of them, but we definitely have to mention the brilliant lectures of L. Bélady, the world-famous former TUB graduate, the software guru, with the title of "Remarks on the likely future consequences of the convergence of computers, communications and consumer electronics", and that of B. Courtois — an author of one of the articles in this issue — about the "State of the Art in CAD". Their lectures gave very interesting pictures of the disciplines where they are among the most famous experts.

About 50 regular workshop presentations from faculty members and students were delivered in the afternoons in the following sessions:

- Engineering Education,
- Computer Aided Engineering,
- Digital Signal Processing,
- Fields and Waves,
- Power Electronics.

It was very good to see the competence of the numerous student presenters, most of their presentations were co-authored by Faculty members. This way members of different departments could get information about the scientific work carried out in other departments, resulting in lively discussions, and hopefully in future collaborations.

Summarizing the effects of the event, besides the immediate effect of gaining useful up-to-date knowledge on the tutorials, I would emphasize this long term effect: learning about each others results and scientific problems can strengthen the links between faculty members of different departments. Since this can positively influence the level of both the education and research on the Faculty, the organizers agreed to repeat the workshop yearly, from now on.

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ACTIVITIES OF THE IEEE HUNGARY SECTION

Technical programmes organised, sponsored or co-sponsored recently by the IEEE Hungary Section are listed in the followings.

Anoyone being interested in the activities of the IEEE (the Instute of Electrical and Electronics Engineers) and/or the IEEE Hungary Section, please, refer to the information published in our January 1992 issue, Vol. XLIII., p.37.

Technical Meetings:

- Image Identification and Restoration (J. Biemond, 16 May 1990)
- Associative Memories via Artificial Neural Networks (A. N. Michel, 22 August 1990)
- The Evolution of U.S. Power Systems (J. A. Casazza, 24 August 1990)
- John von Neumann and the History of Computing (W. Aspray, 4 December 1990)
- Artificial Intelligence and Education – Past, Present and Future (R. A. Aiken, 18 April 1991)
- Last Word in Robot Vision at Present (R. Bajcsy, 29 May 1991)
- Information-Theoretic Asymptotics of Bayes Estimators (A. R. Barron, 1 July 1991)
- Universal Prediction (M. Feder, 3 July 1991)
- Artificial Neural Network and Models of Adaptive Systems (J. Sztipanovits, 3 July 1991)
- Unified Approach to the Stability and Robust Stability Problems (M. Mansour, 23 September 1991)
- Distribution Estimate Consistent in Total Variation (E. C. Meulen, 2 December 1991)
- Projection of Distribution Estimates in Parametric Families (I. Vajda, 3 December 1991)
- Sensory Information Processing in Electric Fish: Computational Rules and their Neuronal Implementation (W. Heilenberg, 27 February 1992)
- Signal Processing with Nonlinear Lossless Dynamic Systems (J. A. Nossek, 22 April 1992)
- Fractals in the Twist and Flip Circuit (L. O. Chua, 22 June 1992)
- On the Separting Capability of Cellular Neural Networks (J. Osuma, 11 December 1992)

Chapter Technical Meetings:

- Optical-Microwave Interactions (7 September 1990)
- Topics in Digital Communication (F.Ivanek, 19 November 1990)
- Application of Optical Fibers in the Distribution Network (F. Tosco, 11 April 1991)
- Hough Transform and it's Use in Digital Image Processing (J. Turan, 30 May 1991)
- Simulation and Design of Nonlinear Microwave Circuits (V. Rizzoli, 16 September 1991)

- Progress and Change in Microwave Radio Communication (F. Ivanek, 22 May 1992)
- Synthesis of State of the Art Linear Amplifiers with "MULTI-MATCH" (P. L. D. Arbie, 17 September 1992)
- Optical Formats for High Speed Networks (I. Chlamtac, 20 January 1993)

Technical Symposia:

- Symmetry of Structure (13-19 August 1989)
- Microcomputer and Microprocessor Applications (17-19 October 1989)
- Brain, Signals and Computers (16-20 October 1989)
- Metropolitan Area Networks (24-25 May 1990)
- Intelligent Measuring Systems (2-4 July 1990)
- Formal Techniques in Programming Technology (28-30 July 1990)
- Reliability and Life-Time of Electrical Machines (1-2 October 1991)
- International Conference on Live Line Maintenance (20-22 May 1992)

IEEE International Conference:

- European Microwave Conference (EuMC) and MICROCOLL (11-14 September 1990)
- International Conference on Harmonics in Power Systems, ICHPS'90 (3-6 October 1990)
- International Conference on Cellular Neural Networks and Applications, CNNA-90 (17-19 December 1990)
- 3rd Mid-European Custom Circuits Conference, CCC-91 (22-24 April 1991)
- IEEE International Conference on Information Theory (23-27 June 1991)
- Reliability in Electronics, RELECTRONIC-91 (26-30 August 1991)
- IEEE International Workshop on Personal, Indoor and Mobile Radio Communication (25-28 May 1992)

Forthcoming IEEE International Conferences:

- IEEE International Symposium on Industrial Electronics, ISIE'93 (1-3 June 1993)
- 6th International Workshop on Atmospheric Icing of Structures, IWAIS'93
- (September 1993) Those who are interested in joining the IEEE Hungary Section, please contact János Bitó (Tungsram TH Co.LTd., H-1340 Budapest). If you have any suggestions concerning the technical programmes (proposals of organising meetings, looking for co-sponsorship of conferences etc.), please, inform Lajos Bálint (Hungarian Academy of Sciences, Nádor u. 7., H-1051 Budapest).

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Information for authors

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Manuscripts should be submitted in two copies to the Editor in chief (see inside front cover). Papers should have a length of up to 30 double-spaced typewritten pages (counting each figure as one page). Each paper must include a 100–200 word abstract at the head of the manuscript. Papers should be accompanied by brief biographies and clear, glossy photographs of the authors.

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Original illustrations should be submitted along the manuscript. All line drawings should be prepared on a white background in black ink. Lettering on drawings should be large enough to be readily legible when the drawing is reduced to one- or two-column width. On figures capital lettering should be used. Photographs should be used sparingly. All photographs must be glossy prints. Figure captions should be typed on a separate sheet.

6th CONFERENCE AND EXHIBITION ON TELEVISION TECHNIQUES

18–20 May 1994, Budapest, Hungary

Organized by the Scientific Society for Telecommunications.

Topics

- TV studio techniques and systems
- Transmission of video and sound signals
- TV transmmitting techniques
- Cable television
- TV reception techniques (TV reception from satellites, antenna systems, TV receivers)
- Measuring instruments and measurement techniques

Announcement of papers is welcome on topics mentioned above with two copies of a one-page A4 format summary before **30th October, 1993** to the address of the Organizing Committee: Scientific Society for Telecommunication, H-1055 Budapest, Kossuth Lajos tér 6-8. HUNGARY, telephone: 36-1-153-1027, fax: 36-1-153-0451 where detailed informations and registration form is also available.

FIRST CALL FOR PAPERS

INTERNATIONAL WORKSHOP ON IMAGE PROCESSING THEORY, METHODOLOGY, SYSTEMS AND APPLICATIONS

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The workshop is open to all aspects of image processing including:

- Image coding, compression, restoration, archivation
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Objectives:

- Invited tutorials providing the state of the art in selected areas
- Presentations containing new, original and unpublished material of research works
- Poster session dedicated to new approaches and applications of fast processing algorithms
- Round table to discuss and present open problems
- Small exhibition

Authors schedule:

Submission of extended abstracts:	15 December, 1993
Notification of acceptance:	30 January, 1994
Camera-ready copy:	15 April, 1994

Mailing address: Prof. Kálmán FAZEKAS
Technical University of Budapest
Dept. of Microwave Telecom.
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- The emerging Eastern European and FSU IT markets within the international context
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INTERNATIONAL SEMINAR ON TELECOMMUNICATIONS SYSTEMS MEASUREMENTS

BUDAPEST, HUNGARY, NOVEMBER 9-10, 1993

Organized by the

SCIENTIFIC SOCIETY FOR TELECOMMUNICATIONS

and the

JOURNAL ON COMMUNICATIONS

The Seminar will give a comprehensive review of measurement problems encountered during installation and operation of modern telecommunications systems and of the measurement methods developed for controlling systems parameters to meet transmission requirements. The speakers will represent Hungarian companies and institutions and outstanding Western system measurement centers having significant relations in Hungary.

Seminar topics include measurement of

- Digital transmission systems
- Synchron digital hierarchies
- Telecommunication protocols
- Digital exchanges
- Digital networks
- Microwave systems
- Optical transducers

A round table discussion will be organized on new measurement methods in developing telecommunications sytems.

Measuring instruments will be presented at an exhibition organized concurrently with the seminar.

Language of the seminar will be English with simoultaneous translation.

Seminar lectures will be published in the October 1993 issue of the Journal on Communications, seminar participants will receive copies of the journal at the registration desk.

Further information

Scientific Society for Telecommunications
Kossuth Lajos tér 6-8.
1055 Budapest, Hungary

Ms Katalin Mitók, organizing secretary
Phone: 36 1 153 1027
Fax: 36 1 153 0451