COMPUTER AIDED CIRCUIT DESIGN

EDITORIAL

It is a great honour for me being able to act as guest editor for the CAD issue of the Journal on Communications just at the 25th anniversary of my first CAD program development. The development of the TRANZ-TRAN (Transistor Transient) nonlinear network simulation program started in 1967, and I am very grateful to my talented coworkers both at the TU Budapest and at Uppsala University for their successful improvements of this program. The development of the TRANZ-TRAN program started earlier than the development of the SPICE program, TRANZ-TRAN is intensively used even today. So TRANZ-TRAN is perhaps one of the computer programs with the longest lifetime.

During this 25 years, a revolutionary change could have been observed in the field of electronics. 25 years ago the electronic equipment were built mostly from discrete components and the digital technique played no important role. Nowadays — excepting several special fields, as for example power electronics — electronic equipment are constructed from LSI and VLSI integrated circuits using mostly digital circuitry.

Naturally, this change has strongly influenced the CAD tools needed by the design engineer. 25 years ago there were only two areas in electronics, where CAD tools were necessary:

- network simulation and
- printed circuit board design.

Nowadays — focusing our interest to the most important field, the digital design — two kinds of engineering tasks are dominating:

- the digital system design using large design program systems and silicon compilers, working by well-developed and maturated cell-libraries, and
- subcircuit design for the cell-libraries or modifying the existing cells of a cell-library for a new semiconductor processing technology. The cell-library contains all information about the cells:
  - the function,
  - the logic scheme,
  - the timing information,
  - the lay-out of the cell including the position of the connection points
  - etc.

The firstly mentioned task is a typical top−down design with a high level of automation. The design starts from a behavioural description and this is converted in several steps into the graphical description of the lay-out. The tools needed for these conversion process are

- hardware description languages, capable of handling information from the behavioural level to the lay-out level,
- programs for hierarchical expansion from higher level to lower level,
- logic simulation programs for checking the timing at the early stage of design (before the lay-out design) and for the post lay-out timing simulation,
- placer and router programs for placing the cells and to realise the interconnections between cells at the lay-out level.

The secondly mentioned task, the cell design is usually some mixture of the top-down and bottom-up designs. The tools needed are the followings:

- network simulation programs,
- logic simulation programs,
- semiconductor device simulator programs,
- process simulation programs,
- lay-out editor programs with design rule checking.

All the above mentioned CAD tools provide a user friendly interface to the designer (window systems, possibilities to follow the design history, graphical input facility, critical chek of the designer activity by warning and error messages, easy-to-use help system, visualization of the results, etc.). These user interfaces make the design work easy and straightforward. The designer can concentrate to his creative activity, and must not use a large part of his time to elude some funny feature of the CAD tools.

It is important to note that the design of an electronic system or an integrated circuit — similarly to all other technical design tasks — has no unique solution. A large number of acceptable solutions exist starting from the fully hardware realization through the partially microprogrammed solution up to the fully software solution, so a growing importantce of the application particial intelligence methods can be expected in the CAD tools, making the decision between the different design variants easier.

The AI methods require large computing power, but the strong interaction between the evolution of computers and CAD tools is well known:

- More efficient CAD tools offer the possibility to develop faster and more efficient computers.
- The fast and efficient computers facilitate the application of more sophisticated CAD tools, and so on...

Finally I must give some historical remarks on the CAD activities in Hungary. It is known, that before the 90-es — caused by embargo restrictions — we were not allowed to buy internationally accepted CAD tools, therefore we had to develop these tools for the Hungarian electronic and semiconductor industry by ourselves. Several groups in research institutes and at the Technical University of Budapest have made valuable contributions to the electronic CAD field.

Dr. Csopaki (TU Budapest) and a group of SzKI developed a hardware description language and a simulation system based on it.

Prof. Csurgay's group (TKI) developed a series of network and logic simulator programs as well as PCB design systems.

Prof. Geher's group (TU Budapest, Inst. for Telecommunication) have reached valuable results in sensitivity analysis program development.

Dr. Javor's group (KFKI) has developed the LOBSTER logic simulation program applying several new ideas in the timing simulation.

Dr. Skultety's group developed network simulation programs with excellent features for analogue design.

Prof. Zombory's group (TU Budapest, Dept. Theoretical Electricity) has interesting results in 2D process simulation, by the HYPREM program.

Finally my department (Dept.Electron Devices, TU Budapest) has developed the previously mentioned TRANZ-TRAN network simulation program, the process simulator STEP, the logic simulator LOG-TRAN, the cell design programs CELL-LIB and CELL-INEX, as well as the THERMANAL program for evaluating the thermal behaviour of integrated circuits and PCB's.

K. TARNAY

Kálmán Tarnay was graduated at the Faculty of Electrical Engineering of the Technical University, Budapest in 1952, receiving the Diploma of Engineering. He received his Dr. techn. degree in 1961 with his thesis concerning the theory of tunnel diodes. In 1966 he received the degree of "Candidate of Technical Sciences" with his thesis about the transient behaviour of field effect devices. In 1983 he received the "Doctor of Technical Sciences" degree of the Hungarian Academy of Sciences.

Since 1952 he has been dealing with research and education in connection to electronic measurements, theory, modeling and computer simulation of electron devices. Until 1959 he was a staff member at the Dept. of Wireless Telecommunication of the Technical University, Budapest. Between 1959 and 1971 he worked at the Central Research Laboratory for Measurements as the head of the semiconductor measurement division. In 1971, he joined the staff of the Dept. of Electron Devices at the Technical University, Budapest as assoc. professor. Since 1984 he is full professor. Between 1977 and 1990 he acted as the head of the department.

He has published more than 140 scientific papers, and he is the author or co-author of many university textbooks, lecture notes and 8 scientific books. He developed one of the first network analysis program, called TRANZ-TRAN, in the second half of the 60-s.

He was invited to various universities as guest professor or guest researcher in the field of theory and modeling of semiconductor devices (e.g. ETH Zürich, Uppsala University, TU Tallin, TU Habana).

In 1983 he recived the "Ph.D. honoris causa" degree from the Faculty of Mathematics and Physics of Uppsala University. In 1989 he was elected as a foreign member to the Finnish Academy of Sciences and Arts.

BEHAVIOURAL SYNTHESIS, PARTITIONING AND ARCHITECTURAL OPTIMIZATION FOR COMPLEX SYSTEMS ON SILICON*

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This paper gives a survey of a new long term project started in June 1989 under the EEC Basic Research program. The interesting set up phase of formulating the project has been presented, showing the way of putting together the know-how of 7 of the leading silicon compiler groups in Europe and their ideas for how design will be done in five years. This could give ideas in planning other research projects and this justifies the early presentation. The project states that logic synthesis and layout synthesis tools are available, but there are no tools for architectural optimization and behavioural synthesis when technology moves to realisation of complex systems on silicon.

The paper gives an overview of the problem, and presents the project plan with descriptions of the sub-projects. Organization and relation to the NORSILC project is mentioned shortly. The paper is referring to works from all partners coordinated by the project manager, Dr. Francky Catthoor, IMEC, who was not able to present the project himself.

1. INTRODUCTION

The research proposed in this project is vital to design future IC's which will contain the equivalent in logic of 16 million memory cells. Currently complex systems are mapped into Silicon starting from an architectural description level. However, the bottle-neck in such megachip designs lies not in realizing the layout from this register-transfer level description, but in mapping the behaviour intended into a suitable architecture. Therefore, in order to fully exploit the integration complexity of future fabrication technologies it is crucial to provide a specification at the highest system level.

Problems related to this change of specification level are fundamental in nature. There are still many domains that are unexplored, where breakthroughs are needed, to make efficient solutions feasible.

Hence there is a need for basic research at different levels on the design trajectory from system to architecture:
1. System definition:

   (a) formal specification of abstract behaviour,
   (b) formal verification of correctness.

2. System partitioning:
   This task involves splitting up the system description into subsystems, each matched to a particular architectural style.

3. Mapping of subsystems into architectures:

   (a) development of synthesis strategies for regular arrays, and co-operating datapaths including architecture exploration,

   (b) investigation of new optimization paradigms for use in synthesis systems such as genetic algorithms and neural nets.

4. Architectural synthesis for the control part:

   (a) Partitioning of a behavioural control description into interacting finite state machines. This involves an architectural optimization.

   (b) Mapping of resulting high-level state machine descriptions in hardware, e.g. by means of a process independent multilevel logic framework.

Seven partners with complementary expertise have decided to combine and co-ordinate their efforts to tackle this major task. They will identify basic shortcomings at each of these levels and then attempt to provide fundamentally new ways of approaching them. Efficiency in terms of throughput, chip-area and memory will be an important objective. In addition, the resulting IC designs should *comply with the bandwidth, power and pin-count limitations of VLSI components*. This work is of crucial importance for future designs in domains as speech, image-processing, video, vision, telecommunication, factory automation, advanced process control, biomedical technology, radar, sonar and so on.

2. OBJECTIVES AND ADVANCE

Currently, complex systems are mapped into silicon from an architectural description level. Existing design tools do not offer the possibility to synthesize architectures from a higher-level specification. However, in order to fully exploit the integration complexities of future fabrication technologies, it is critical to start from a specification at a highest system level and use formal synthesis methods. It is expected that high level "silicon compilation" techniques will incorporate 50% of all designs in the next decade. Problems related to this change of specification level are fundamental. There are still many domains that are unexplored, where breakthroughs are needed to make efficient solutions feasible.

Hence, the goal of this project is to develop and evaluate new techniques for behavioural synthesis, partitioning, and architectural optimization for such complex systems.

The partners in this project gather a large experience in silicon compilation. Each of them has a major contribution

in this domain as they are heading five important research projects in Europe on the subject.

The final goal is to provide the basic tiles to pave a complete path from specification to architecture. We aim at "true" silicon compilation which allows for several mapping and architectural approaches and which handles a broad class of applications. The workpackages proposed in this project are research programs that have to lead to fundamentally novel techniques which tackle the bottle-necks in the current approaches. The results will be directly useful to construct new tools in ESPRIT type projects which are more industrially oriented.
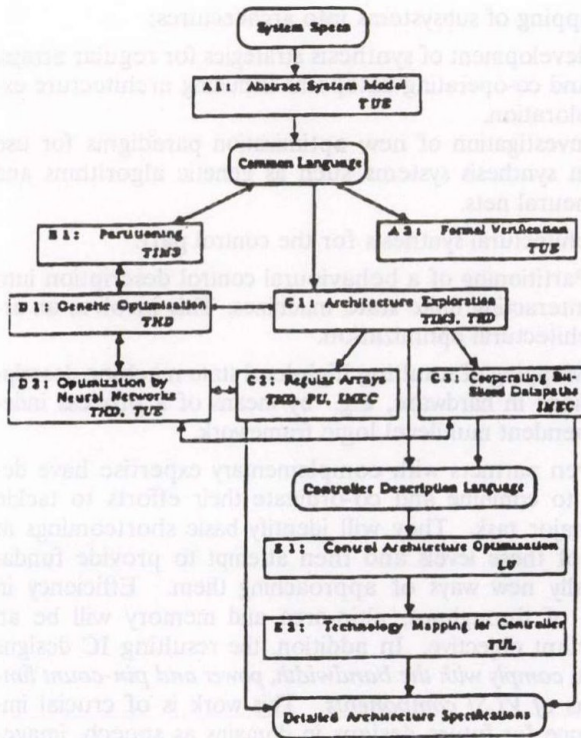

Figure 1. Behavioural synthesis, partitioning and architectural optimization for complex systems on silicon

2.1. System specification and formal verification

Synthesis and formal verification need an appropriate unified abstract system model that allows for flexible specification of behaviour and that has an unambiuous meaning for the synthesis and verification processes. Note that this does not imply a unified system definition language. It is more appropriate to see the system model as a global mechanism, very much like a finite state machine, a Turing machine or a Petri net, yet capturing both the aspects of data dependency and concurrency (control) in a general sense. The research will study the relation between abstract system model documentations and various applications.

The first step of synthesis is performed by projection mechanisms that map the abstract system model into application specific descriptions (closer to the realisation). The projection mechanisms will be subject to theoretical

and experimental investigations regarding their nature and complexity. The essential novel feature of the abstract system model will be that it establishes a general basis for formal verification against application specific requirements. This will be done by extracting those features relevant for the verification task thereby reducing the complexity of the verification problem. We will study the complexity of both the extraction and the actual verification mechanisms theoretically and experimentally.

2.2. System partitioning

The main goal of the research in this task is the construction of a behavioural partitioning scheme that can produce efficient designs for complex systems from a behavioural description.

The weakness of today's behavioural silicon compilation is the low performance of the automatically produced circuits. In this task, we will address efficient partitioning schemes for complex systems, and high level architecture optimization methods in order to alleviate the problem.

Since the architecture will be generated automatically, we need a new generation of architectural optimization tools that allow the user to make architectural trade offs. Such tools will be interactive in a first phase. The final goal is to have an intelligent design system able to fulfill automatically a set of constraints concerning speed, area, and power.

2.3. Mapping of subsystems into architecture

In this work package, synthesis strategies for implementing complex (signal) processing systems in an application-specific way will be addressed. We expect that a knowledge-based approach is required where the formal rules have to be embedded in an efficient framework. This is especially needed because we want to achieve a high flexibility in terms of extensibility and user-interaction. However, the work in task D on other paradigms than expert system will be taken into account too in the course of the project.

We will look into several architectural styles. This requires architectural exploration techniques to identify the best suited strategies. In this project, we will concentrate on high-throughput applications where the requirements are even more stringent than for medium rates. For this purpose, powerful architectural constructs such as pipelining, parallel resources, distributed storage, multiple busses and hierarchical control will be investigated.

1. For the modular high-speed subtasks, regular array architectures such as pipelined or broadcast (SIMD) organizations will be studied. We will consider nested as well as non-nested loops, straight as well as conditional code. Moreover, we will put a lot of emphasis on the mapping of the initial behavioural description into uniform recurrence equations.
2. A second important architectural style for high-throughput ASIC systems is the co-operating bit-sliced datapaths steered by a hierarchically decomposed controller. Instead of only looking at simple data-path units, we will have a detailed look at applications which require a more complex control unit, which is hierarchically organized or partitioned in order to save area. Especially the sometimes very complicated initalization and the off-chip communication subtasks have to be incorporated.

2.4. Optimization Framework

One of the goals of this project is to map complex systems which are defined on a high level description onto architectures that can be easily transformed onto silicon. Within this process various optimization problems from a wide spectrum have to be solved i.e. partitioning and mapping problems which are of crucial importance for this step. Although dedicated heuristics have been developed for these complex problems, no efficient and accurate optimization strategy with general validity is known. Within this work package we focus our interest to new optimization methods, that promise the cited requirements.

1. Dynamic network approaches as a result of adaptive learning mechanisms with special emphasis to neural networks and the Boltzmann machine.
2. Genetic algorithms for which exploration is still at the beginning. The effectiveness of a combination of these different techniques will be studied too. As a result a general valid optimization framework for the use in task B and C will be delivered.

2.5. Architectural control flow synthesis

Most VLSI systems contain one or several control units. For instance, in task C, very complex descriptions will have to be dealt with for the co-operating data-path approach. Such control units may also be provided by an automatic partitioning system as discussed in task B.

The general problem of designing optimal and efficient control units is much less known than the corresponding problem for the data-paths. The main goal of the research is to find automatically the optimal organization of a given control unit starting from an architecturally independent description. The important problem has not been solved yet in current systems. For the subsequent logic synthesis and minimisation known methods can be used. However, in the optimization a number of critical restrictions must be fulfilled concerned with timing and scheduling based on data-flow dependencies. Such performance criteria are not satisfactorily solved by the current systems.

The optimal choice of the control unit organization may potentially result in a substantial reduction of the required total area in silicon, in addition to the area gained by subsequent logic synthesis that can be based on e.g. multi-level logic optimization. In order to provide an efficient technology mapping, a framework of flexible and process independent module generators based on expert system techniques and symbolic layout will be applied.

3. PROJECT ORGANIZATION

Figure 2 shows the project organization. This is based on the principle of putting the existing competence in groups together and find coverage for the whole field. Many other ESPRIT projects are made so distributed that you do not get any real co-operation. But in this project the number of partners is limited and the level of competence is comparable as nearly all have been involved in developing their own silicon compiler and therefore have background in design at the lower level where silicon compilers are now.
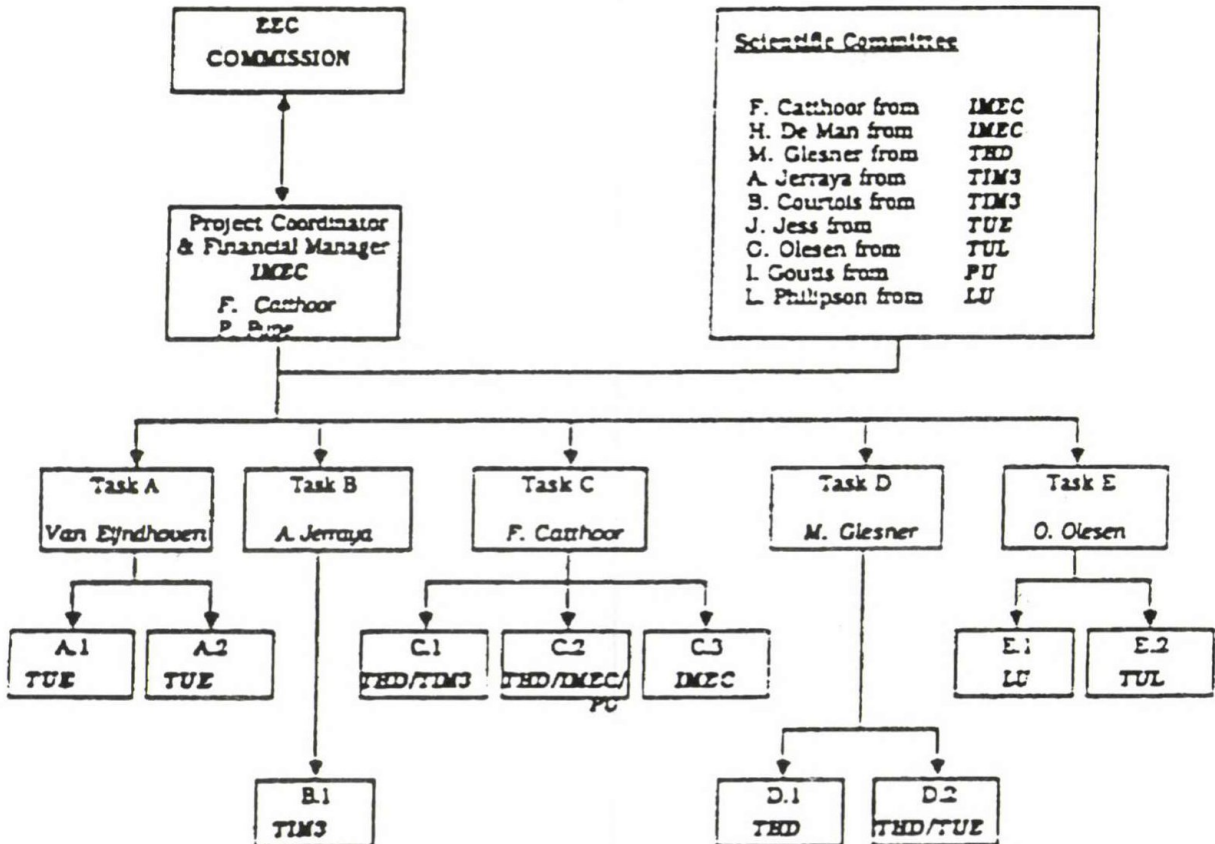

Figure 2. Behavioural synthesis, partitioning and architectural optimization for complex systems on silicon

The names of the key projects from the different groups are:

IMEC   Cathedral
THD   Algic
Tim 3   Syco
TUE   Sagantec (commercial name)
TUL   Catoe
LU   Movie

4. NORDIC PARTICIPATION

As can be seen the Lund and Lyngby universities are the Nordic participants. This is due to the fact that under project planning only a limited number could be accepted and the two groups had the work that fitted best to the project plan. The know-how obtained from ASCIS is to some extent used in the NORSILC-II project.

5. CONCLUSION

Without showing actual research results this paper gives an overview of a very important long term basic research.

By combining the know-how of seven strong groups a strong plan for a four year project with 14 full-time engineers at Ph.D. level has been formulated and documented with 98 references. The key issues are architectural synthesis and partitioning, but many other topics are also dealt with. It seems that this project will be one of the leading European projects that will form an important step towards the goal: Automated synthesis of system design into chips.

6. ACKNOWLEDGEMENT

The editor would like to thank all partners in the ASCIS project for the inspiring co-operation in the start-up phase of this project. The key names are mentioned in Fig. 2.

Especially, the project manager, Dr. Francky Catthoor, IMEC, should be mentioned.

REFERENCES

As this is a survey paper the only references given is an internal report: "Technical annex for ESPRIT Basic Research Action 3281". This contains 98 secondary references.
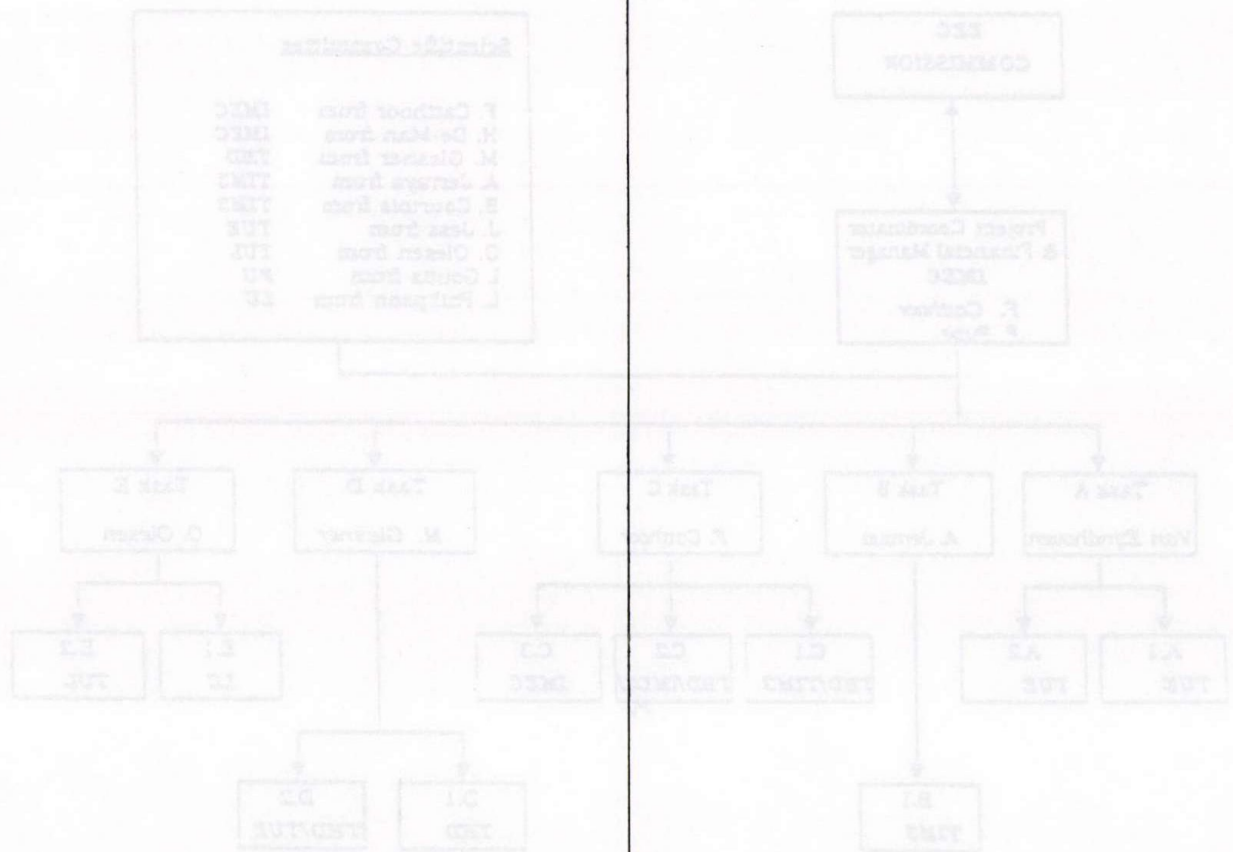
MULTILEVEL SPECIFICATION OF DIGITAL SYSTEMS WITH HARDWARE DESCRIPTION LANGUAGES

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The well-known top–down approach to design development and verification does not depend on any particular hardware description language. However, its usefulness and effectiveness depends on the degree of support provided by the hardware description language for separate abstract specification, and definition of hierarchy between abstract specifications and implementations. Designers will not use a methodology if the language support is inadequate so that the methodology is complex and demanding.

1. INTRODUCTION

The fast growing complexity of digital systems to be designed has increased the demand for computer aid in all phases of the design process [1]. Investigations have been made and results achieved in simulation of hardware units for early detection of design errors but results are not widespread in practice [2]. The simulation methods are not too popular due to the following reasons:

- restrictions in hardware description languages,
- operating of the simulated unit is possible only at the lowest level, but a large system can not be described at gate level,
- notions, structures and relations of simulation are not popular with development engineers,
- high efforts are needed on the user-side for application,
- the lack of completeness in the CAD system between the functional or the logical description and the structural phase of design process.

We think we should support the designer's work with a very flexible system, which gives him assistance when formulating his own ideas, syntactically and semantically controls the concepts, documents and archivates every detail of the design process and transforms the results automatically into the input forms of the existing CAD systems. Now a hardware description language will be presented which is developed for a multilevel system, that applies top – down approach in digital systems' synthesis.

2. DESIGN PROCESS IN THE MULTILEVEL DESCRIPTION SYSTEM

The design process in CARS (Computer Aid for Recoursive Synthesis) consists of three steps to be repeated recoursively [3], [4]:

- the user describes the behaviour of units with time parameters. This description is called functional specificaiton, and refers only to inputs and outputs. CARS checks the syntax;

- the user describes the proposed structure of this unit using the functional specification of the components and the interconnections among them. CARS checks the syntax;
- the user executes the simulation process on the functional unit and on the structure with the same input data. CARS compares the results of the simulation on the functional specification and the structure;
- if the structure fulfils the requirements the procedure may be repeated for the components of the structure. When all the functional specifications are the descriptions of existing units, the design process is finished.

2.1. Comparative Simulation

A designer usually verifies a design in some form of simulation. This task often requires the designer to manually compare the simulation result with an informal design specification. Occasionally, the designer also has a high level behavioural description (written in, for exmple, C or Pascal) whose output can be compared to the output of the simulator. The design is simulated using a set of test vectors, the behavioural model is run on the same test vectors, and the results are compared.

While this process of verification is adequate for simple designs, as designs become more complex it becomes less satisfactory. It is limited to the extent in which the designer is still able to debug a new design. It assumes a "black box" view of the design unit (or entity) in which the entity is accessible only through its ports.

Our model of design checking is based on utilizing a separate entity specification to generate constraints on the input of the entity, the internal state, and the output. Input constraints allow the simulator to check if an entity is being used correctly. For example, if the setup or hold time on a signal is not met, the entity can report an input constraint violation. This helps the designer to spot the source of timing errors instead of having to trace the source of the error back from the simulation result. Output constraints behave like the post simulation comparison previously described, with the addition that they may be executed dynamically, during the simulation.

Support tools for comparative simulation will check the simulation results for the functional specification and for the structure.

3. THE FEATURES AND ELEMENTS OF HARDWARE DESCRIPTION LANGUAGE

The description language makes possible, for the designner to describe the behaviour and the structure of a system

at any level of the design process. The most important requirements are that [1]−[4]:

- the language should provide the description of unit as functional specification at any level and provide the definition of the structure by the components (lower level functional units) and their interconnections;
- the language elements and procedures provided should be level independent;
- the description of the functional specification and its structure should be a document of this unit;
- the elements of the language should provide the time correct description of the units;
- it should be possible to apply formal proof techniques to prove that the design satisfies the requirements.

In the next part of this article we will present the language elements developed for the CARS system [3], [4].

3.1. Description of the behaviour

The behaviour of functional units can be described as a functional specification. In the language the functional specification is called TYPE. A type is identified by an identifier. The type identifier is succeded by the formal parameters; by the external input, output and bus signal identifiers, i.e. strings beginning with letters and containing letters and digits.

For example:

```
TYPE: ADDER (A,B,CI,S,CO.)
ADDER is here the type identifier;
A,B,CI,S,CO are formal parameters;
```

The user defines the external connections and the behaviour algorithm in the body of a type. The external connections are signals, grouped as inputs, outputs and busses. They can be described by identifiers. These identifiers have attributes, as width in bits, realization and representation of the signal values and limitations for set of values. The realization of outputs and busses can be totem pole, open-collector and tristate. The direction for busses can be defined as bidirectional or output. In the general declaration part:

```
INPUTS;  <signal declarations>.
OUTPUTS; <signal declarations>.
BUSSES;  <signal declarations>.
```

The <signal declaration> part is a list of signal declarations separated by semicolons. All signals, having the same attributes can be declared together by listing their names, separated by commas and putting the common attributes after the names. Accordingly, the form of a general signal declaration is:

```
<signal names> <width> BITS, <digit number>
               <representation> DIGIT,
               <output type> <bus direction>
               EXCEPT (<exception list>)
```

The <width> and <digit number> are decimal numbers, the <representation> can be either BIN (binary), OCT (octal), DEC (decimal) or HEX (hexadecimal), while <bus direction> can be BIDIRECTIONAL or OUTPUT. The <output type> and <bus direction> parts can be used only for output or bus signals. The <exception list> is a list of numbers or intervals, that specifies the prohibited values for the declared signals.

For example:

```
INPUTS:  A,B 4 BITS, 1 HEX DIGIT; CI
OUTPUTS: S   4 BITS, 1 HEX DIGIT; CO
```

The signals are defined for a 4-bit binary adder, the length of the A and B input signal is four bits and CI (carry input) input signal is one bit long. When the length of signals is not specified, the default option is one bit. The representation is hexadecimal for the A and B input signals. For the S output signal the default option is binary. Both the input changes and the responses take the form of input and output events, respectively. Events are changes in the value of a signal. An input event consists of an identifier and the description of changes forming the event. The change description consists of a signal identifier and the value taken by the given signal.

This is the form of an input event:

```
<event name>:<signal name>CHANGES_TO<value>
```

The language allows the reference of any input signals by name or subsets of these signals, by using the ANY or ALL keyword together with the INPUTS or BUSSES signal type description. The change description can refer to one or more signals and to any value.

For example:

```
INPUT_EVENTS: ARISE: A CHANGES_TO 1;
              INCHG: ANY_INPUTS CHANGE;
              ALLCHG: ALL_INPUTS CHANGE_TO 1;
              BCHG: B CHANGES.
```

Output events are responses for the input events changing the value of one or more output signals. An output event takes place if any input event triggers it, and certain time dependent conditions are met. The time of the output event is expressed by a delay time from the triggering event.

The form of an output event is as follows:

```
<event name>: AT <time>, IF  <condition>,
                                    <effect>
```

The <time> consists of an input event name reference and conditionally a delay time. The time restrictions can refer to setup and hold time and to constant value of signals.

For example:

```
FLOPSET: AT CLKRISE+40 NSEC,
         IF D=1 FROM CLKRISE-10 NSEC
                    TO CLKRISE+5  NSEC,
         Q=1
```

This example describes the setting of an edge triggered D flip-flop. The Q output signal takes the value 1 after 40 nsec of the CLKRISE input event. The value assignment takes place only after the D input signal satisfies the 10 nsec setup and the 5 nsec hold time condition. The condition part may be more complex and the effect part may consist of many assignments. At the left side of the assignments the signal reference may be indexed or not indexed, and at the right side of the assignment a logic assignment may be referring to any declared signals or to any constant. The effect part may consist of memory read and memory write operations. If there are many output events depending on the same condition, this may be declared separately as a common condition. Common conditions may

be nested without any restrictions. A type may consist of any input, output and bus signal, any input event and any output event. There are no restrictions for the complexity of the condition or the effect part.

As an example, the description of the behaviour of a D flip-flop is given below:

```
TYPE: DFLOP (D, CP, CL, PR, Q, NQ).
INPUTS: D, CP, CL, PR.
OUTPUTS: Q, NQ.
INPUT_ EVENTS:
     CPRISE: CP CHANGES_TO 1 BIN;
     CLFALL: CL CHANGES_TO 0 BIN;
     PRFALL: PR CHANGES_TO 0 BIN.
OUTPUT_EVENTS:
     SET:    AT CPRISE+33 NSEC,
             IF D STEADY FROM CPRISE-20 NSEC
                         TO   CPRISE+5  NSEC
                 AND CL=1 BIN AND PR=1 BIN,
             Q=D, NQ= NOT D;
     CLEAR:  AT CLFALL+33 NSEC,
             Q=0 BIN, NQ=1 BIN;
     PRESET: AT PRFALL+33 NSEC,
             Q=1 BIN, NQ=0 BIN.
DFLOP END.
```

In this example it can be seen that the type description gives nothing about the internal structure of the described object. It is only a real functional specification.

3.2. Language elements for simplification

If a designer does not know the exact time when the output signals get their values, he or she can use a time interval in which the values of the actual output signals are not available. The name of this element is operation.

The structure of an operation is as follows:

```
<operation identifier>:<time and condition>
                     <effect part>
      <operation identifier> END.
```

The prefix <operation identifier>, and the <operation identifier> END flank the description body. In the <time and condition> part the start and stop time specifications can be specified.

The form of the start and stop specifications:

```
STARTS_AT      <time expression>, <condition>
TERMINATES_AT <time expression> OR <condition>
```

If the condition part is specified, the operation will be executed only if the condition is met. If stop is specified with a condition, the execution of the operation, specified by the effect part, will be ended if this condition is met.

The form of the effect part is as follows:

```
<normal effect part>, <early stop part>
```

In the normal effect part there are assignments specifying the value of the signals at stop time. The values of these signals are unavailable during the operation time. When the operation is completed because of the condition in the stop specification, the values of signals referred in the effect part take the values specified in the early stop part of the assignments. In the effect part the next statements can be used: simple assignments, if statements, ON statements and memory operation. On the right side of

the simple assignments arithmetical and logical operators may be specified. The IF statement consists of one or two simple assignments and a condition. If the condition is met the first simple assignment (after the THEN keyword) will be executed, otherwise the second one (after the ELSE keyword). In the ON statement more assignments may be given. Depending on the value of the referred variable the appropriate assignment will be executed. In the top — down design process not only TYPES are decomposed into STRUCTURES but OPERATIONS are decomposed into lower level OPERATIONS and/or EVENTS as well. This feature of the language helps the designer to make time refinements. Nevertheless the bottom-up approach is also supported by the operation concept since different event and/or operations can be composed into a higher level operation, thus eliminating unimportant details of timing considerations at a particular level.

Example for operations:

```
TYPE: ADDER (A,B, CI, CO, S).
INPUTS: A, B 4 BITS, 1 HEX DIGIT; CI.
OUTPUTS: S 4 BITS, 1 HEX DIGIT; CO.
INPUT_EVENTS: CHG: ANY_INPUTS CHANGE.
OPERATIONS: SUM: STARTS_AT CHG
                 TERMINATES_AT CHG+24 NSEC;
                 RESULT: S=A+B+CI.
            SUM END.
            CRY: STARTS_AT CHG+16 NSEC;
                 TERMINATES_AT CHG+16 NSEC;
            RESULT:
       IF (A+B+CI)>=10000 BIN THEN CO=1 BIN;
       IF (A+B+CI)< 10000 BIN THEN CO=0 BIN.
            CRY END.
OPERATIONS END.
ADDER END.
```

3.3. Description of the structure

The structure description has name, input and output connections and elements. The external connections must be declared as INPUTS, OUTPUTS and BUSSES. After the signal declarations, the structure has two lists: the list of elements constituting the structure and the list of connections among the elements. The elements of structures are realized by types, and since more elements may be realized by the same type, the actual realization is regarded as copies of that particular type. The copies are identified by proper names indicating the actual place of use and parameters.

The form of the element list is as follows:

```
ELEMENTS:  <type identifier>:<copy list>
```

The types listed in this element list are component types of the given structure and their level is considered lower than the level of the actual structure. The parameters for a given copy in the element list correspond to those in the type definition. The signal names as formal parameters in the element list may coincide with the names of the input or output signals or with parameters of other elements in the list. In both cases the system automatically connects all the terminals concerned. This is an implicit definition of the connection. The connection list defines all the remaining nets in the structure. A net definition is a list of connected signals separated by the concatenation (−)

mark. The designer may refer to any subset of a multi-bit wide signal by using subscribed identifiers.

The form of the connection list is as follows:

```
CONNECTION: <list of nets>
```

where `<list of nets>` is the definition of all the nets separated by semicolons. In this explicit case of definition the inputs and outputs of the components have to be identified by a qualified identifier:

```
<element name>.<name of signal in type>
```

The qualified identifier may be subscripted, too.

An example for a structure, describing the structure of a BCD adder is given below:

```
STRUCTURE BCDF.
INPUTS: A, B 4 BITS, 1 DEC DIGIT; CI.
OUTPUTS: S 4 BITS, 1 DEC DIGIT; CO.
ELEMENTS: ADDER: ADD1(A,6 DEC,0 BIN, * , * ),
                 ADD2(*,B ,CI , * , S ),
                 ADD3(*,* ,0 BIN, * , S );
          INV: INV1(*,*).
CONNECTIONS: ADD2.S- ADD3.A,
             ADD2.CO-INV1.A-CO,
             INV1.Y- ADD3.B(1)-ADD3.B(3),
             ADD3.B(0)-ADD3.B(2)-0 BIN.
BCDF END.
```

In this example ADD1, ADD2, ADD3 are the names of copies of ADDER, which is a four bit binary full adder.

4. TEST PROCEDURE

Let us consider two descriptions of the same system. One is the functional specification (behavioural description), a type, the other is a structural one, a structure. Let us assume that all the elements in the structure are defined, thus both type and structure can be tested by sim-

ulation, using the same input data. The results of the two tests must be identical if the model is correct. This comparison is the last step of the process. A test set is specified by the type description since it must contain all functions expected from the given type. On the other hand the structure may contain additional unspecified functions, too. This way a positive result of the comparison does not mean the identity of the type and the structure, it is indicating only that the structure fulfils the specified requirements. If the same structure is tested for a different type description, as it is necessary in bottom-up approaches, it may or may not fulfil additional or changed requirements. The comparison means the evaluation, whether the set of events describing the behaviour of the type is a complete subset of the possible events of the respective structure.

This evaluation may be performed at different levels. Obviously the evaluation on the lowest level is easy, because only the numeric result-values of the simulation must be compared, but simulation must be done for all the possible values and combinations of inputs within the region of the specified input value set.

5. CONCLUSIONS

The specification method and the hardware description language described in this article was developed for the CARS system. The system CARS has been developed to assist the designer in the synthesis phase of the digital system design. CARS applies a top-down structured approach in the design process and can be used at any user defined level of refinement. CARS does not pose any restriction on the creative work of the designer, but gives means to describe his concepts and tools to check his results. The design method and the language developed are well suited to describe the behavioural concepts and structures as well. One of the most important feature is that the designer can use the same language elements for the behavioural and for the structural description.

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Gyula Csopaki was born in 1946 in Kölcse, Hungary. He received the M.Sc. degree in telecommunication systems from the Technical University of Budapest, Hungary, in 1969, and the Ph.D. degree in computer science from the Hungarian Academy of Sciences in 1987. Since 1969 he has been working at the Institute of Communication Electronics, Faculty of Electrical Engineering. Technical University of Budapest. He is now an associate professor, and his research interests are in computer aided design of digital systems, CHDL and telecommunication software design.

UPGRADED EDUCATION OF IC DESIGN METHODOLOGY AT THE DEPARTMENT OF ELECTRON DEVICES OF TUB

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The paper deals with the education of CAD in microelectronics at the department of Electron Devices, Technical University of Budapest. First the results achieved up to now are discussed then the progress of the development based on a TEMPUS Joint European Project is detailed. Finally some of the outcome of this TEMPUS JEP is presented.

1. INTRODUCTION

Our department has always put a great emphasis on the education of CAD methods and tools. We have been dealing with the education of the different issues of circuit and logic level simulation for 23 years already and for the last 15 years we have been dealing with questions of computer aided IC design. Seven years ago, when the curricula of the Faculty of Electrical Engineering were reformed, we insisted on starting a new educational direction, the so called branch of microelectronics and technology. In this branch of education, in the particular field of microelectronics, there are about 30 students being educated at our department. We have 4-5 postgraduate students with different doctoral scholarhips.

In the curriculum reform we put a great emphasis on the topics of microelectronics design and CAD. The most important subjects in this field (together with the semester hours per week) are summarized in Table 1.

Table 1. CAD related subjects and their semester hours

Subject	6.sem.	7.sem.	8.sem.	9.sem.
Computer-aided design	3	3		
Microelectronics		8	5	
Circuit constr. & technology			3	4
Project laboratory		2	5	5

Since 1991 our circumstances and possibilities have changed significantly and this enabled us a further progress in the education of CAD. One important aspect is, that our department won a grant for a Joint European Project in the frames of the TEMPUS program of the EC, which allows a great upgrade in the hardware platform and software tools used in our CAD education and allows an in-crease of our international relationships in this field. Another aspect is, that our upgraded CAD education matches well the latest changes in the curriculum structure of the Hungarian higher education. Namely we think that all of our CAD related subjects should be rather attractive as selectable subjects in the second half of the studies at the Faculty of Electrical Engineering of TUB.

2. CAD EDUCATION – UP TO NOW

In the past 6-7 years the base of our educational activities was a VAX-750 computer, which has been completed recently with 2 VAX Station 3100 computers and with a MicroVAX 3100/20 to form a VAX Cluster. Today we have 42 seats (lots of terminals, PC-s and workstations) in our local area network which allows an easy access to our VAX computers and the university wide computing services. In our computer laboratory there are 20 terminals accessible for our students. Out of these 20 there are 10 terminals with graphics capabilities (PC-s with Tektronix terminal emulation ranging from standard EGA resolution to special high resolution displays well suited for layout design.) The VAX configuration is completed with hardcopy devices: 2 plotters and a laser printer.

Until 1991 we had to be satisfied with software tools mainly of domestic development. We have a circuit simulation program and a thermal simulation package for IC-s (both of them were developed at our department) [1], we have a logic simulator, a layout editor, a DRC program, a layout extractor and some other utilities, such as CIF or GDSII compilers, etc.
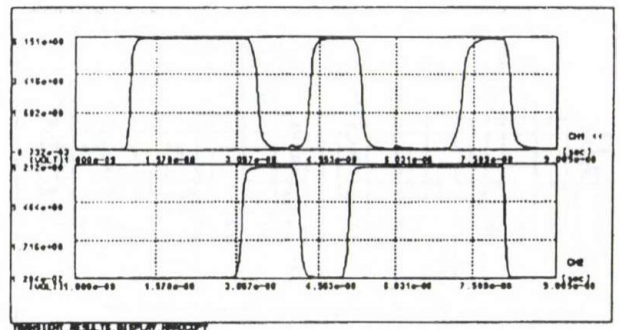

Figure 1. Results of the transient simulation of the circuit of Figure 3 using the TRANS-TRAN program

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The students have spent most of the time of the CAD course in the computer laboratory. From the educational, didactical point of view we always emphasized, that every student had an own, individual task to be solved and for the work every student had an own platform (terminal, PC). With the above hardware basis this goal could be met with an appropriate weekly time schedule.

Another focus of our education is the field of computer graphics. The students are provided with separate practices where they can experience the usage of different graphics devices. Most of the applied design programs are graphic-interactive, see Figures 1. and 2.
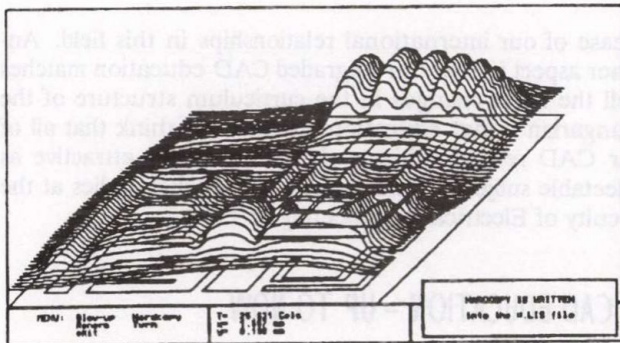
Figure 2. Temperature distribution on the surface of a monolithic IC. The calculations were performed using the THERMANAL program

The main tasks of the practices are as follows:

- Usage of the different versions of our circuit simulation program [2], [1]. Hierarchical circuit description. Definition of macro models (subcircuits) and their application. Effect of the modification of device parameters. (The circuits to be investigated are the ones, that were studied in the Microelectronics courses; these are mainly MOS IC circuits, see eg. Figure 3).

- Register level, functional and gate level simulation with the appropriate programs.

- Layout editing with a graphic editor. Hierarchical design: cell design and application of a cell library.

- Layout verification with DRC and netlist extraction.

- Thermal verification with thermal simulation.
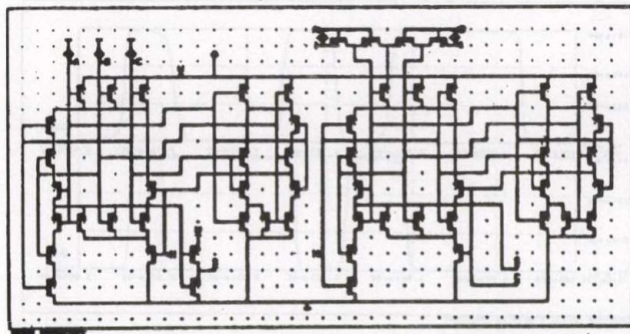
Figure 3. Transistor level realization of binary adder during the editing phase of the PC version of the TRANS-TRAN circuit simulation program

These are standard tasks to be performed by every student. They give more or less experience enough for the further usage of the necessary CAD tools in subsequent subjects and in solving the project laboratory tasks.

In the individual projects (in the project laboratory) a part of the students designs an IC detail or they design even a complete integrated circuit. From didactical point of view we find necessary that the most successful designs should be realized. Until 1991 we had no processing possibility, but since that year we started submitting the best students' designs for processing in MPC runs. The first design — still produced with our old design tools — has been realized using the NORCHIP MPC facility in the spring of 1991. The layout of this chip can be seen in Figure 4.
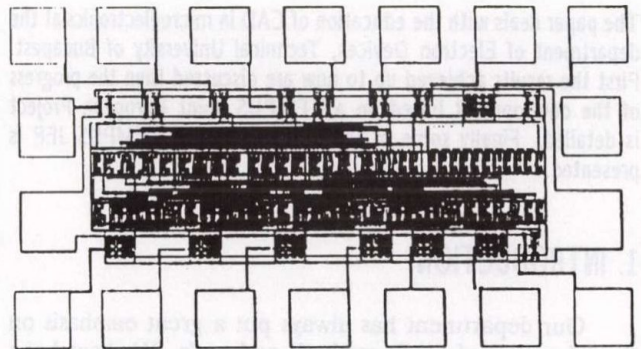

Figure 4. Layout of a 4-bit binary up−down counter. The chip was designed in 1990-91 using our old design tools and it was manufactured at the NORCHIP MPC facility using a 1,2 µm CMOS process

3. REFORM OF THE CAD EDUCATION

The microelectronics CAD is a field, where major updates are needed in every 5-6 years both in the hardware platforms and in the software tools. This upgrade at our department is made possible by a TEMPUS Joint European Project approved for 1991 and extended to 1992.

The title of our TEMPUS JEP is *Cooperation, curriculum development and training in the field of microelectronics design methodologies*. Our West-European partners are:

- Institut für Mikroelektronik, TH Darmstadt,
- IMEC (Inter University Microelectronics Center), Leuven,
- Microelectronics Center, Danish Technical University,
- Institut National Polytechnique de Grenoble.

From the TEMPUS grant we bought 4 SUN workstations in 1991, and we also bought the majority of the software tools recommended by EUROCHIP. (EUROCHIP is a consortium of 5 West-European research institutes and universities in order to form a service organization that helps with recommendations its member institutions — there are about 400 universities in the EC which are EUROCHIP members — and provides them with certain hardware and software tools at special discount prices and represents all the member universities at

the chip manufacturers by organizing a substantial number of multi project chip (MPC) runs. By a special tempus-EUROCHIP membership our department also represents the Technical University of Budapest in this service organization.) In the autumn of 1991 we started making a shift towards the new facilities provided by EUROCHIP. In particular: we bought some software tools, such as the *Cadence Edge Design Framework* for standard cell an full custom IC design, the *SOLO 1400* standard cell IC design system of ES2, the *HILO* logic level and the *HSPICE* circuit level simulators, which run partly on our new SUN machines and partly on our VAX machines.

Besides the tempus-EUROCHIP membership, our western partners contribute to our facilities upgrade by organizing short courses in every year at our location in order to prepare the entire staff of the department for taking the full advantage of the new equipment and design tools. These courses are open for the colleagues working at other departments of our faculty as well.

Our goals within our TEMPUS JEP can be summarized as follows. We want

- to meet the West-European standards in education of IC design and to keep our position at this level,
- to assure that the best students' designs are realized in MPC runs in an increasing number,
- to assure for the best students a semester-abroad program or a diploma work at one of our western partners on a regular basis.

Certain elements of the software tools that we recently bought should replace the programs that were used up to now. For example the *MODEL* hardware description language of the *SOLO 1400* system is well suited for using it in an elementary CAD course as well. Doing so gives the advantage, that in later CAD related subjects (eg. in project laboratory) the students can use this tool in a real IC design environment, such that they are already familiar with it.

4. THE FIRST RESULTS

An important point in our facilities upgrade is that it must be performed such that the running, regular CAD courses must not be disturbed, while our staff-members and an increasing number of students must get acquainted with the new tools. This contradiction was solved by the help of our western partners. In the summer vacation of 1991 our staff-members made themselves familiar with the new design programs, while 6—8 of our students were and are provided with semester abroad programs, practical training and diploma works at our West-European partner institutions.

Since some of our people already gained practice in IC design using the new tools, the first results did not delay.

The first chip designed with the *Cadence Edge Design Framework* using the 1.5 μm CMOS cell library of ES2 has been manufactured already utilizing the services of the EUROCHIP consortium. Recently we received the ready chips and according to the first tests they operate properly. This circuit was designed in the summer of 1991 by one of our students under the control of his Hungarian supervisor at one of our western partners (see Figure 5.).
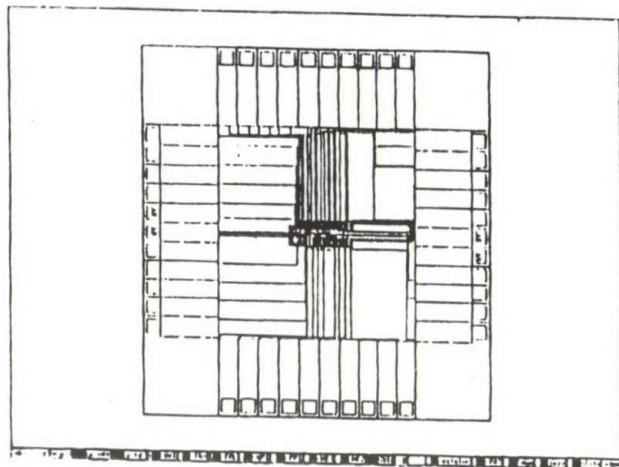

Figure 5. Floorplan of a special multiplexer chip designed by one of our students using the Cadence Edge Design Framework with the SOLO configuration. The circuit has been manufactured using the MPC service of EUROCHIP

Of course our activities were not restricted to the summer training. In September of 1991 various projects were set up that might result in realized chips. One of these projects is a digital control system for model railways. There are two 5-th year students participating in the project. They started the specification of the system and building the analog circuit environment of their planned chips in the framework of their project laboratory work. During the system specification they relied on the 1.5 μm CMOS cell library of ES2 which is accessible both in the *SOLO 1400* system and in the *Cadence* system. Now they continue the work as a diploma project. Since the *SOLO 1400* system arrived at our department in January of 1992, the project is recently in the logic design phase and by April of 1992 the manufacturing of the designed chips is expected. A status report of this project can be found in this proceedings [3]. There is another design project which is focused on the realization of a special purpose image processing chip.

These two projects should result in 3 chips in 1992. We expect about 3-4 projects of similar complexity in every year that would be finally realized in the form of a multi project chip — giving our students the feeling of performing a complete engineering task.

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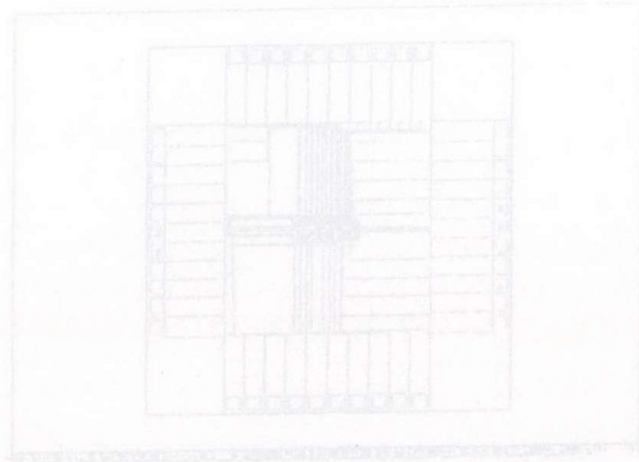[2] V. Székely, "Thermal problems of semiconductor devices", Ph.D. dissertation, Budapest, 1968, in Hungarian.
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Dr. Székely has published his theoretical and practical results in more than 80 technical papers.

Marta Kerecsen-Rencz graduated at the Faculty of Electrical Engineering of the Technical University of Budapest in 1972, receiving the Diploma of Electrical Engineering. She received her Ph.D. degree in 1980 for her thesis about Linvill Type Bipolar Transistor Modelling.
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In 1989/90 he worked at IMEC in Lueven, Belgium. His field of interest is computer aided IC design, network simulation and device simulation.

Individual Papers

SOME PROBLEMS IN THE DESIGN
OF A HITLESS SWITCH

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In digital communications systems applying switching-type diversity, the switching process has to be "hitless", i.e. no bits should be omitted or repeated during the switch-over process. This involves various synchronization tasks: the clock has to be synchronized so that no excess jitter occurs and the delay difference of the two sequences has to be eliminated. The hang-up phenomenon is dealt with, and a clock synchronizer, free of this problem and yielding acceptable jitter is described. Furthermore, the input jitter tolerance and the synchronization problem of random bit sequences are dealt with, and performance parameters are analyzed. It is shown that random sequences can be synchronized even if the error probability of one or both sequences is very high. The mentioned problems will be solved assuming a hitless switch device discussed in [7]. Some of the problems dealt with here are described in more detail in [5], [8], [9].

1. INTRODUCTION

Diversity systems play a key role in microwave and recently also in optical communications systems. Space, frequency and angle-diversity are applied in microwave systems, while phase and polarization diversity in optical communications. Switching-type diversity is the most appropriate if one diversity route deserves more than one transmission path, it is, however, often applied in 1/1 systems as well. In digital communications systems, switching has to be "hitless", i.e. no bits should be omitted or repeated during switch-over, or "errorless", if error correcting coding is applied. While diversity switching is relatively free of problems of analog communications, the hitless or errorless requirement creates several problems in digital transmission.

Many digital communications systems are equipped with hitless switches, and general descriptions also exist [e. g. 1,2]. There are at least two synchronization problems which according to the knowledge of the authors, were not previously dealt with in detail:

- clock synchronization, free of the hang-up phenomenon and not causing excess jitter,
- synchronization of random bit sequences.

This paper presents a summary and extension of the results published in [5], [7], [8], [9]. In Section 2, the hang-up phenomenon is dealt with and a hang-up free design described. Section 3 deals with the design of the main blocks of this sub-system. In Section 4, the input jitter tolerance of the main blocks is investigated. The synchronization problem of random bit sequences is defined in Section 5, and the appropriate algorithm is given. Section 6 contains the analysis of error-free and noisy transmission.

2. CLOCK SYNCHRONIZATION IN DIVERSITY SWITCHING

The delay difference between the input data streams feeding the switch have to be eliminated in order to obtain hitless switch-over. First we deal with the theoretical operation of the switching system, and the demand for fraction-period clock synchronization is discussed later.
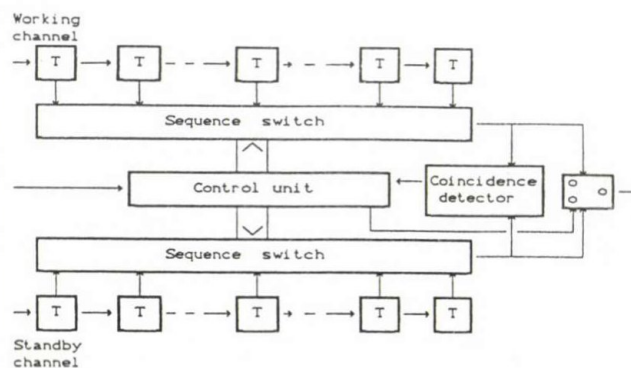

Fig. 1. The shift register model of delay equalization

Shift registers can be used for delay equalization as shown in Fig. 1. Let us assume that the output is connected to the central tap of the shift register in the working channel. In the standby channel, the output of the sequence switch should be connected to the appropriate tap of the shift register in accordance with the delay difference. After switching, the output tap is probably shifted from the central position according to the actually existing delay difference. At the next switching event, the connection point can be shifted further, and sooner or later, any shift register of finite length will become insufficient to perform perfect hitless switching: the switch "hangs-up".

To prove this we have to keep in mind that in most cases, switch-over from the working channel to the standby happens while the former is highly distorted and the latter not; at switching back, however, transfer characteristic of both channels are approximately equal. If we assume that during the first switching operation, the output tap of the standby shift register is the i-th (the center tap being the 0-th), it is highly probable that the output tap of the working channel shift register at switch-back will be the i-th as well. The situation is similar at the second, the third etc. pair of switching operations. The mathematical model of this process is thus a random walk with absorbing boundaries (as the shift register length is finite). Absorption here occurs with probability one.

Using a so-called elastic memory rather than a shift register for delaying the signals, the hang-up problem discussed above can be avoided, and this also provides the fraction-period clock synchronization without having to use any other circuits. When an elastic memory is applied, the delay between its input and output can be changed by varying the phase difference between the writing and reading clock signals because of its writing and reading clock signals may be different.

Detailed description of such a hitless switch can be found in [7], and a simplified block diagram of this switch is shown in Fig. 2.
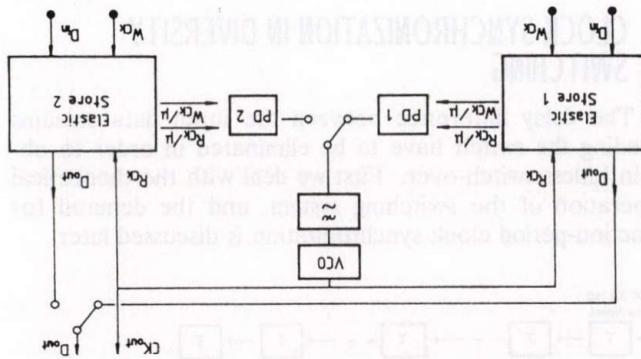
Fig. 2. Simplified functional diagram of a hitless switch

The output signal is provided by one of the two elastic memory units. (In calculations, the elastic store shown in Fig. 3 will be assumed.)
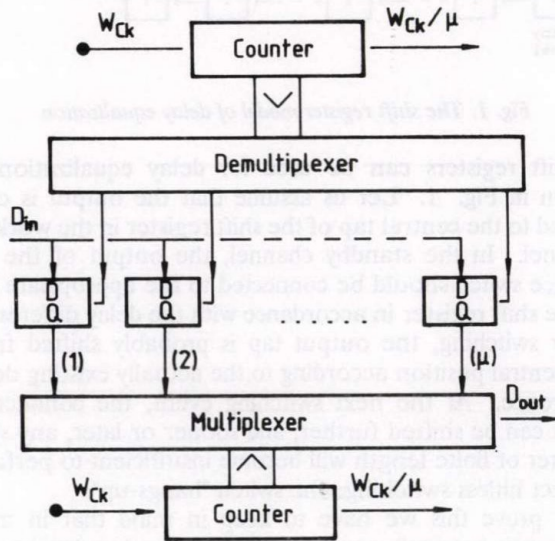
Fig. 3. Elastic store block

To avoid uncertainty of the output signal, the reading and writing counters have to address different flip-flops. Maximal safety can be obtained by maintaining the maximal phase shift between the writing and reading counters. In this case, the maximum tolerable delay difference between incoming signals (measured in clock period) is half of the number of flip-flops.

The required phase condition can be obtained and maintained by using a PLL. At the switching instant, the PLL

is switched to the standby channel too. Although in the standby channel there can be some phase error (due to the delay difference between input signals), the PLL will reduce it, and the perfect phase condition will be restored.

3. BASIC DESIGN OF THE PLL

During and after the switching process, the magnitude of the jitter must remain within given limits. Jitter and wander specifications are given in CCITT Recommendation G.823. Jitter is defined as the short term variations of the significant instants of a digital signal with regard to their ideal positions in time. According to the definition given in the cited recommendation, the meaning of the jitter is almost identical with that of the phase fluctuation. The instantaneous value of jitter can be measured by using an appropriate weighting band-pass filter. The transfer function of this filter, specified in G.823, can be seen in Fig. 4.
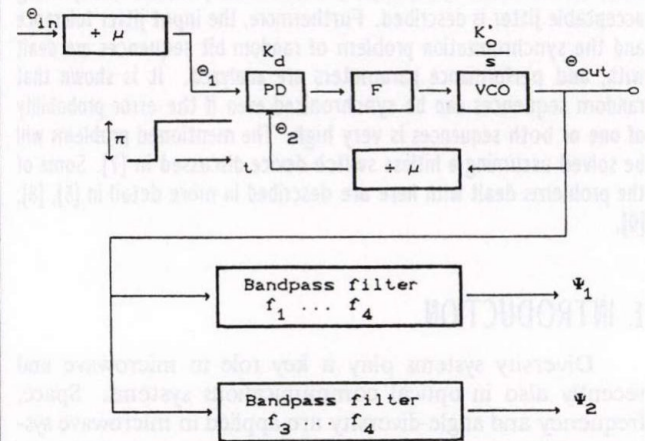

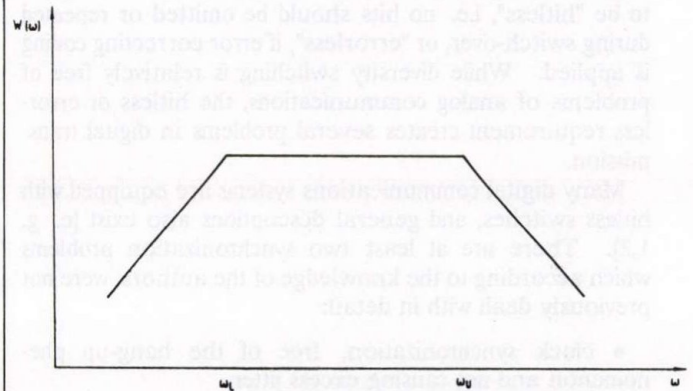*Fig. 4. Band-pass filter transfer function for output jitter test*

Fig. 5. Model of the PLL under jitter test

Let us consider the theoretical model of the PLL under jitter test to obtain its transfer function (Fig. 5). 1.5 UI and 0.075 UI are the limits of permissible peak-to-peak jitter when the lower cutoff frequencies of the weighting filter are 200 Hz and 10 kHz, respectively, at 140 Mbit/s bit rate. The upper cutoff frequency is 3500 kHz. The output

phase is μ times Θ_2 due to dividing. The worst case in sensing the jitter is at the phase step of π:

$$\Theta_{\text{out}}(s) = \mu\Theta_2(s) = \frac{\mu\pi}{s}H(s) \qquad (1)$$

where $H(s)$ is the well-known phase transfer function of the PLL, and μ is the division ratio of the counter which has to be equal to the number of the flip-flops.

The phase transfer function of a PLL is

$$H(s) = \frac{\Theta_2(s)}{\Theta_1(s)} = \frac{K_0 K_d F(s)}{s + K_0 K_d F(s)} \qquad (2)$$

where $F(s)$ is the transfer function of the loop filter and K_d is the phase discriminator gain. The equivalent gain of the VCO in the system is given by

$$K_0 = \frac{K_0'}{\mu} \qquad (3)$$

where K_0' is the VCO gain in rad/s/V.

Now we are interested in calculating the output jitter denoted by ψ in Fig. 4. The jitter is originated from the phase fluctuation by a linear transformation and is measured in UI (unit interval). For this reason, the phase fluctuation has to be transformed by the appropriate weighting filter and related to the whole period (2π radians):

$$\Psi(s) = \frac{1}{2\pi}\Theta_{\text{out}}(s)W(s) \qquad (4)$$

where $W(s)$ is the transfer function of the weighting band-pass filter given by

$$W(s) = \frac{s}{s + \omega_L}\frac{\omega_U}{s + \omega_U} \qquad (5)$$

ω_L and ω_U are the lower and upper cutoff frequencies, respectively. Substituting (5) and (1) into (4) we have

$$\Psi(s) = \frac{\mu}{2s}H(s)W(s) \qquad (6)$$

First we are going to investigate the behaviour of a first-order PLL. In a first-order PLL, there is no loop filter at all, and its phase transfer function is given by

$$H(s) = \frac{\Theta_2(s)}{\Theta_1(s)} = \frac{K_0 K_d}{s + K_0 K_d} \qquad (7)$$

Substituting (5) and (7) into (6) we have

$$\Psi(s) = \frac{\mu K_d K_0 \omega_U}{2(s + K_d K_0)(s + \omega_L)(s + \omega_U)} \qquad (8)$$

The jitter response to a phase step of π is

$$\psi(t) = A_K e^{-K_d K_0 t} + A_L e^{-\omega_L t} + A_U e^{-\omega_U t} \qquad (9)$$

where

$$A_K = \frac{\mu K_d K_0 \omega_U}{2} \cdot$$
$$\cdot \frac{1}{(K_d K_0 - \omega_L)(K_d K_0 - \omega_U)} \qquad (10)$$

$$A_L = \frac{\mu K_d K_0 \omega_U}{2} \cdot$$
$$\cdot \frac{1}{(\omega_L - K_d K_0)(\omega_L - \omega_U)} \qquad (11)$$

$$A_U = \frac{\mu K_d K_0 \omega_U}{2} \cdot$$
$$\cdot \frac{1}{(\omega_U - K_d K_0)(\omega_U - \omega_L)} \qquad (12)$$

The calculated jitter functions are shown in Fig. 6. The peak-to-peak jitter does not exceed the limit if the loop gain $K_d \cdot K_0$ is smaller than about 400/s.
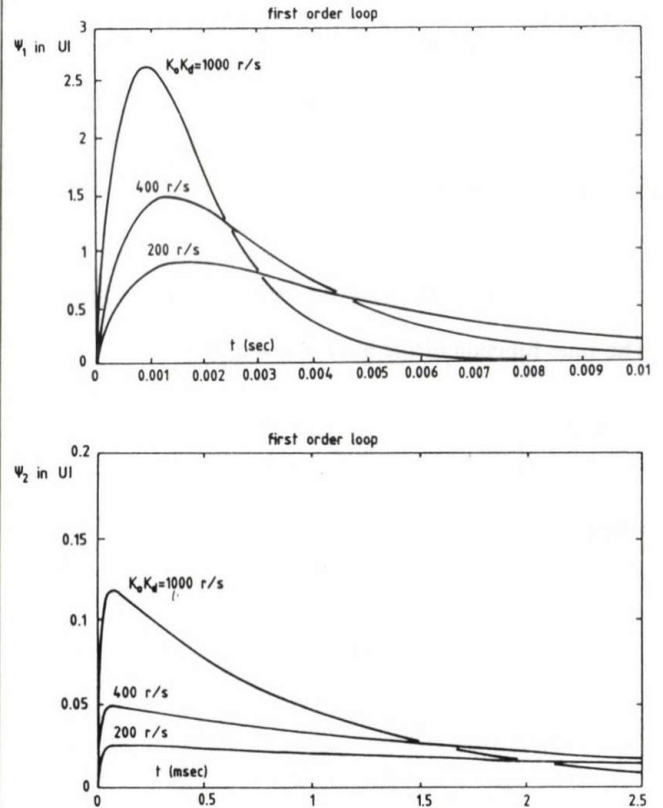

Fig. 6. Jitter time functions of a first-order PLL

On the other hand, the static phase error has to be as low as a few degrees. If the static phase error were large, greater than π/μ, the writing counter could not address the corresponding flip-flop, therefore the tolerable delay would be decreased. The static phase error of a first-order PLL is given by

$$\Theta_e = \frac{\Delta\omega}{K_d K_0} \qquad (13)$$

where $\Delta\omega$ is 2π times the difference between the incoming signal frequency and the VCO free-running frequency. Assuming $\Delta\omega$ of $2\pi \times 1000$ rad/s, the phase difference is 15.7 radians. Therefore a first-order PLL is not suitable to control the clock synchronization in a hitless switch in spite of the fact that during operation, phase-jumps rather than frequency jumps occur. Thus a second-order PLL is needed, being discussed in the following.

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In control theory, it is common practice to write the denominator of a second-order transfer function in normalized form:

$$\text{Denominator} = s^2 + 2\zeta\omega_n s + \omega_n^2 \qquad (14)$$

where ω_n is the natural frequency and ζ is the damping factor. We are going to deal with the so-called high-gain loop when satisfying the condition

$$K_d K_0 \gg \omega_n. \qquad (15)$$

In this case, the phase transfer function can be approximated as

$$H(s) = \frac{2s\zeta\omega_n + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (16)$$

Substituting Eqs. (16) and (5) into Eq. (6), we obtain

$$\Psi(s) = \frac{\mu\omega_n\omega_U}{2} \cdot$$
$$\cdot \frac{2s\zeta + \omega_n}{(s^2 + 2\zeta\omega_n s + \omega^2)(s + \omega_L)(s + \omega_U)} \qquad (17)$$

The time function of the jitter is given by

$$\psi(t) = A_c e^{-\delta t}\cos(\beta t) + A_s e^{-\delta t}\sin(\beta t) + $$
$$+ A_L e^{-\omega_L t} + A_U e^{-\omega_U t} \qquad (18)$$

where

$$\delta = \zeta\omega_n \qquad (19)$$

$$\beta = \omega_n\sqrt{1 - \zeta^2} \qquad (20)$$

$$A_c = \mu\omega_n\omega_U \cdot$$
$$\cdot \text{Re}\, \frac{2\beta\zeta + (\omega_n - 2\delta\zeta)j}{2\beta(\omega_L - \delta - j\beta)(\omega_U - \delta - j\beta)} \qquad (21)$$

$$A_s = \mu\omega_n\omega_U \cdot$$
$$\cdot \text{Im}\, \frac{2\beta\zeta + (\omega_n - 2\delta\zeta)j}{2\beta(\omega_L - \delta - j\beta)(\omega_U - \delta - j\beta)} \qquad (22)$$

$$A_L = \frac{\omega_n + 2\zeta\omega_L}{(\omega_L^2 - 2\zeta\omega_n\omega_L + \omega_n^2)(\omega_L - \omega_U)} \qquad (23)$$

$$A_U = \frac{\omega_n + 2\zeta\omega_U}{(\omega_U^2 - 2\zeta\omega_n\omega_U + \omega_n^2)(\omega_U - \omega_L)} \qquad (24)$$

The calculated functions are shown in Fig. 7. We can observe that the natural angular frequency must be lower than 500 rad/s. In order to provide this value, a VCXO rather than a free-running VCO has to be applied. On the other hand, the steady-state phase error can be neglected when a high-gain second-order PLL is used.
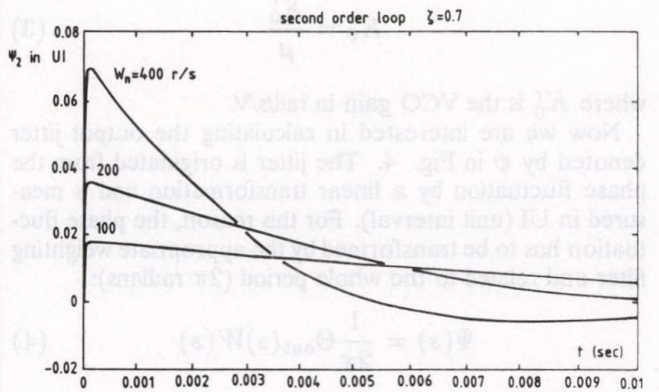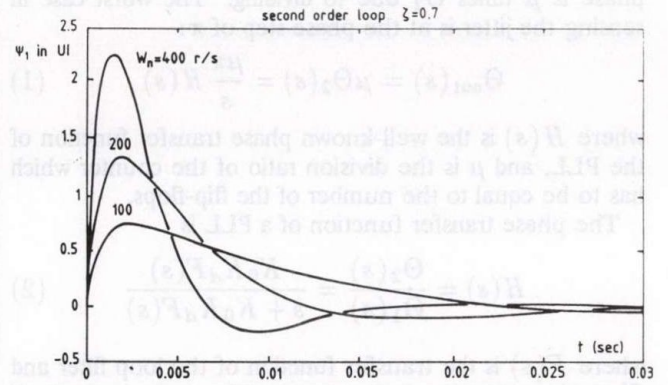

Fig. 7. Jitter time functions of a second-order PLL

4. DESIGN OF THE PLL TAKING INTO ACCOUNT THE INPUT JITTER

Besides of output jitter, input jitter tolerance is a parameter of digital communication equipment as well, so the input jitter tolerance of such a hitless switch has to be determined. According to the recommendation [6], for convenience of testing the required input jitter tolerance is defined in terms of the amplitude and frequency of sinusoidal jitter, which, when modulating a test pattern, should not cause any degradation in the operation of the equipment. Let us see what causes operation error in the hitless switch. In spite of that the hitless switch being a three-port device, we shall assume a two-port device for the input jitter tolerance test, with no switchover command allowed during the test.

In this special case, our system consists of an elastic store and a PLL having parameters already determined above. Errors can emerge if a particular flip-flop is simultaneously addressed by the reading and writing process. As mentioned above, the PLL tries to hold the maximum distance between these two flip-flops. Furthermore, the PLL in a hitless switch has to have a narrow bandwidth. If the input signal is corrupted by jitter of relatively high frequency, in our case by a sinusoidal one, the PLL will not follow the input signal fluctuation, so the flip-flops being read and written get closer and closer. As long as they do not coincide the input jitter will simply be transferred to the output.

On the other hand if they do coincide then a bit error can occur. To avoid this, the length of the elastic memory has to be greater than the peak-to-peak value of the "addressing error" caused by jitter. The tolerance scheme for the lower limit of the maximum tolerable sinusoidal input jitter is given in [6]. To calculate the maximum tolerable input jitter of the hitless switch, we have to use the well-known error transfer function of the PLL:

$$H_e(s) = \frac{\Theta_{\text{in}} - \Theta_{\text{out}}}{\Theta_{\text{in}}} = 1 - H(s) = \frac{\Theta_e}{\Theta_{\text{in}}} \qquad (25)$$

Furthermore

$$|H_e(s)| = \frac{A_e}{A_{\text{in}}} \qquad (26)$$

where A_e is the difference between the input and output jitter amplitudes, and A_{in} is the input jitter amplitude in terms of unit interval UI.

Our task is to determine an A_{in} for a given A_e that does not introduce the error mentioned above. (If A_e is greater than or equal to the number of flip-flops in the elastic store, the flip-flops being written and read can coincide.) Let us express A_{in} as

$$A_{\text{in}} = \left| A_e \frac{1}{1 - H(s)} \right| \qquad (27)$$

Applying a second-order PLL with a so-called high-gain loop,

$$A_{\text{in}} = \left| A_e \omega_n^2 \frac{1 + 2\zeta \frac{s}{\omega_n} + \frac{s}{\omega_n^2}}{s^2} \right| \qquad (28)$$

To satisfy the recommendation, a suitable choice of A_e and ω_n is required. Taking the results, $\omega_n = 200$ rad/s and $\zeta = 0.7$, into account, A_e has to be as high as 7. This means that we have to use a 14 bit longer elastic store! To shorten that length, another ω_n and ζ should be found. Recalculating the output jitter as detailed in Section 3, $\omega_n = 100$ rad/s and $\zeta = 2$ satisfy the requirements as well. Substituting these numbers into the expression of A_{in} (28), $A_e = 5$ is high enough to satisfy the requirements as shown in Fig. 8. The upper curve is the input jitter amplitude that causes ± 5 bit difference between the writing and reading clock of the elastic store, and the lower curve is the recommended lower limit of maximum tolerable input jitter amplitude. The curve of the input jitter tolerance of the hitless switch meets the qualitative expectations because as it can be seen in Fig. 8, the PLL can follow the jitter having a frequency lower than ω_n but, of course, not the jitter having a higher frequency. Increasing or decreasing the PLL bandwidth causes opposite effects in output and input jitter tolerance, so an optimum bandwidth exists.
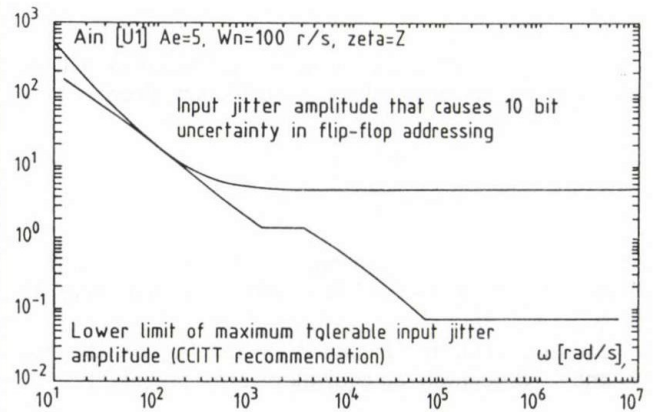

Fig. 8. Input jitter tolerance

In Table 1, parameters of the PLL satisfying the requirements of CCITT recommendation are given.

Table 1. Parameters of the PLL satisfying the requirements of CCITT recommendation, from the input and output jitter point of view

$\frac{\omega_n}{r/s}$	100	125	150	175	200	225	250	300
ζ	2	1.6	1.3	1.1	0.9	0.7	0.6	0.4
A_e [UI]	5	5	5	5	6	6	7	8

As we have seen, $A_e = 5$ is a good choice. This means ± 5 bit uncertainty in addressing the flip-flops so it results in shortening the usable length of the elastic store by 10 bits! This result may be dramatic considering that the maximum delay difference in a 140 Mbit/s system is about 10 bits. Consequently, we have to apply a two times longer elastic store. This means that not only the maximum delay difference has to be taken into account in the elastic store length determination but the above mentioned phenomena as well.

5. SYNCHRONIZATION OF RANDOM BIT SEQUENCES: PROBLEM STATEMENT

Sequence synchronization is one of the classical problems of digital communications. In usual code-synchronization, either the code structures are synchronizable by themselves or periodically inserted frame-synchronizing words are available. The very broad subject of code-, word- and frame-synchronization is dealt with in myriads of papers, some recent ones being [3] and [4]. In the present situation, random bit sequences have to be synchronized: there are two identical or (in the case of nonzero error probability) nearly identical sequences; their structure, however, is unknown, with given source statistics; synchronization means here the measurement of their delay difference and the alignment of this difference. Actually it will be assumed that the source is an equiprobable random one, justified by the presence of a scrambler which is, for various reasons, always applied.

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5.1. Definitions

Two identical or nearly identical bit sequences will be said to be of low delay difference if for any given $\varepsilon > 0$ there exists an M for which

$$\sum_{|D|>M} P_D \leq \varepsilon \qquad (29)$$

where P_D means the probability of a given delay difference. They are of bounded delay difference, if a finite M exists for $\varepsilon = 0$.

Assuming error probabilities P_{E1} and P_{E2} for the two channels, respectively, an equivalent error probability

$$P_E = P_{E1} + P_{E2} - 2P_{E1}P_{E2} \qquad (30)$$

can be defined. There are two performance measures of the synchronization operation: P_N, the probability of not finding synchronism and P_F, that of finding it in a false position. The sequences are said to be synchronizable in the statistical sense if for any δ and S_0 exists with

$$\left.\begin{array}{l} P_N \leq \delta \\ P_F \leq \delta \end{array}\right\} \; ; \; S \geq S_0 \qquad (31)$$

where S is the number of bits investigated; actually S is the synchronizing delay.

Let $s(n)$ be one of the sequences and $s'(n)$ the other. Then

$$s'(n) = s(n + D)$$

or

$$\qquad (32)$$

$$s'(n) \cong s(n + D)$$

for error free or errored channels, respectively. In achieving synchronization, we have to insert K bits of delay, resulting (for the error free case) in

$$s''(n) = s'(n + K) = s(n + D + K) \qquad (33)$$

i.e.

$$s''(n) = s(n) \quad \text{if} \quad K = -D \qquad (34)$$

In this case, the sequences are said to be synchronized.

5.2. The synchronizing algorithm

According to Section 2, there are $\pm M$ bits available in the finite-length elastic store which can be inserted sequentially. If decision is made on "synchronism found", the standby switch can be operated. If decision is made on "no synchronism", one bit delay has to be inserted and observation started. The following decision rule is than appropriate:

• decide on "synchronism found" if there are at most m differences between the two sequences during N bits;

• decide on "no synchronism" as soon as the number of differences counts $m + 1$.

It has to be determined whether the sequences are the sequences synchronizable at all in the statistical sense, particularly under highly errored conditions?

If so, what are the appropriate values of m and N, given P_E and specified P_F and P_N?

And finally, what are the statistical properties of the synchronizing delay?

6. SYNCHRONIZATION OF RANDOM BIT SEQUENCES: DISCUSSION

6.1. The possibility of synchronization

The following theorem holds:
Two random bit sequences originating from a given source can be synchronized in the statistical sense if and only if

i. their delay difference is low, and
ii. the error probability is less than 0.5.

Part i. draws the attention to the fact that some a-priori knowledge about the channel behaviour is essential in order to decide on the synchronizability of the channels in a practical case. Part ii., on the other hand, shows that errors do not make synchronization impossible. This second part is, of course, not self-evident, as in the case of increasing error probability, the number of errors (i.e. the number of differences in the two sequences) within a particular sequence of length N increases; thus m, the admitted number of differences has to be increased as well, needing a further increase in N. The Theorem is proved in [5].

6.2. Design of the sequence synchronizer

The appropriate values of N, m and M have to be determined. For the error-free situation, it is shown in [5] that

$$A/2 \leq P_F < A \; ; \; |D| \leq M \qquad (35)$$

with

$$A = \frac{M(3M + 2)}{2M + 1} 2^{-N} \qquad (35a)$$

and

$$N = \log_2 \frac{M(3M + 2)}{2M + 1} - \log_2 P_F \qquad (36)$$

For nonzero error probability, the followings can be written:

$$P_N = 1 - \sum_{i=0}^{m} \binom{N}{i} P_E^i (1 - P_E)^{N-i};$$

$$|D| \leq M \qquad (37)$$

and

$$P_F < 2^{-N} \frac{M(3M + 2)}{2M + 1} \sum_{i=0}^{m} \binom{N}{i} \qquad (38)$$

The first of these is simply the probability of having more than m errors if the probability of error is P_E. The second

gives the false detection probability by taking (35) and the nonzero magnitude of m into account. With (37) and (38) the appropriate N and m can be determined by successive approximation. Some figures are given in Table 2. To choose an appropriate value for M, i.e. the maximum alignable delay difference, an a-priori knowledge about the channel behaviour is essential; if this is available, an appropriate value for ε has to be chosen, and the corresponding M determined. In practice, taking 140 Mbit/sec transmission into acocunt, $M = 5 - 10$ is sufficient. For higher bit rates, M can be assumed to vary proportionally to this.

Table 2. Parameters of a sequence synchronizer with given performance parameters and channel error probability

M	5								99	
P_N	10^{-6}				10^{-3}				10^{-6}	
P_F	10^{-6}		10^{-3}		10^{-6}		10^{-3}		10^{-6}	
P_E	N	m	N	m	N	m	N	m	N	m
10^{-8}	23	0	13	0	23	0	13	0	27	0
10^{-6}	28	1	18	1	23	0	13	0	33	1
10^{-4}	32	2	21	2	28	1	18	1	37	2
10^{-2}	47	6	31	5	36	3	25	3	52	6

6.3. Statistics of the synchronizing delay

Taking the search algorithm as described in the previous Section into account, the synchronizing delay (S) can be given as

$$S = N + \sum_{j=0}^{J} t_j \qquad (39)$$

Here J is a random variable, uniformly distributed in the range of $\pm M$; t_j is also a random variable with a probability of

$$P(t_j) = 1/2 . \text{ Pr } [m \text{ differences among } t_j - i \text{ bits}]$$

This probability can be determined by simple combinatorial analysis if we take into account that the event in brackets above occurs if $r + s - u = m$, where r is the number of differences in the error-free sequences, and s and u are the numbers of errors among the $t_j - r - 1$

corresponding bits and among the r different bits, respectively. The result is

$$P(t_j) = 2^{-t_j} \sum_{i=0}^{m} \binom{t_j - 1}{m - i} .$$

$$\cdot \sum_{l=0}^{m-i} \binom{t_j - 1 - m + i}{l + i} . \qquad (40)$$

$$\cdot \binom{m - i}{l} P_E^{2l+i} (1 - P_E)^{t-1+2l-i}$$

Taking Eq. (39) and the above result into account, the probability of a particular value of S can be determined applying again combinatorial analysis. Due to the very complex formulae, only the expected value of S for the noiseless case will be given. This can be determined by the application of Wald's formula:

$$E(S) = N + E(t_j) \cdot E(J) = N + 2M(m + 1) \quad (41)$$

If P_E is nonzero though small, the errors have no great influence on $E(S)$.

7. CONCLUSIONS

It has been shown that a hang-up free hitless switch can be designed by the application of an appropriate PLL; design formulae are given leading to requirements which can only be fulfilled if a VCXO in applied. Further it has been stated that random bit sequences can be synchronized if their delay difference is low (as defined in the paper) and an a-priori knowledge about the delay difference is available. If an observation period long enough is available, there is no limit on the error probability.

In practical cases e.g. for $P_E < 10^{-2}$ the synchronization delay is in the order of 100. Consequently, sequence synchronization doesn't pose any limit on the operation speed of the switching system, at least in high capacity digital radio, as the time constant of quality degrading is not less than 1 to 10 msec.

With the application of the methods described, a hitless switch subsystem has been designed and built. Practical measurements have proved the applicability of these methods. Some practical points and results are desribed in [7].

ACKNOWLEDGMENT

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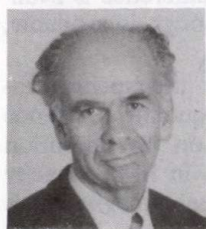
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FFT BASED QPSK CARRIER RECOVERY

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A novel frequency detector considerably extending the acquisition range of carrier recovery loops in digital communication systems is presented. The proposed method needs the performance of a few-point FFT algorithm, and combined with frequency sweeping techniques, enables very fast acquisition.

1. INTRODUCTION

In continuous-mode QPSK satellite modems [1] the frequency error of the carrier can be as high as the Nyquist frequency of the digital transmission. Traditional carrier synchronizers overcome this large frequency-offset by applying loops involving phase and frequency detectors in parallel [2].

A well-known example of the conventional frequency detector (FD) is the balanced quadricorrelator [3]. In this configuration, the loop behaviour is governed by the FD during acquisition, and by the phase detector (PD) in steady state. Once lock is acquired, the FD has to be switched off to reduce the steady state phase jitter. For QPSK satellite modems, a quadricorrelator aided four-phase decision-feedback loop (FDFL) was designed and examined in [11].

In a feed-forward structure, the FD can operate on the QPSK modulated signal rather than the baseband one [4], [5]. This configuration is used in this paper but the FD is based on a new concept.

In another configuration, conventional PD's are transformed into phase/frequency detectors (PFD) which behave as frequency detectors during acquisition and phase detectors at steady state [6].

The Fast Fourier Transformation (FFT), an efficient algorithm for digital signal processing, has recently appeared as an alternative solution of synchronization problems [7], [8]. The idea of [7] is to use FFT instead of a filter-bank but details are not presented. The method described in [8] is given in more detail.

The FFT block is working in a loop, and the error signal is derived from the instantaneous powers of the in-phase and quadrature-phase baseband signals. The solution, however, can only be used for DBPSK signals if the FFT operation is synchronized with the bit timing interval.

The application of the FFT presents many problems. The most important problem is the inverse proportional relation between the frequency resolution and the computational load.

For continous-mode QPSK satellite modems, we propose a new frequency detector based on the FFT algorithm which has good performance and reasonable computational complexity.

2. FFT FREQUENCY DETECTOR

To understand the basic idea, consider for simplicity the BPSK signal shown in Fig. 1. Let us apply a rectangular window which matches a single symbol time interval T. Performing an FFT operation on the samples taken from this window, the result contains only one spectral component at the carrier frequency because the periodic extension of the sequence is a perfect sinusoidal signal. In the implementations where the symbol timing clock is not available for carrier synchronizers, the spectrum is distorted because the samples to be transformed are taken from a window which has an arbitrary initial time instant. Distortion increases if the signal is bandlimited and noisy. Since the problem is not tractable mathematically, the analysis was carried out by computer simulation. Results showed that quite good carrier estimate can be achieved if the samples are taken from two symbol windows and using a few-point FFT (e.g. $N_{FFT} = 128$) [12].

Fig. 1. BPSK signal

The algorithm for estimating the carrier frequency of noisy QPSK signals is the following (see Fig. 2).
- Sampling of the noisy, bandlimited QPSK signal.
- Gathering samples from a 2T interval.
- Performing a few-point FFT algorithm. (If the number of points in the FFT is higher than the number of samples, then samples are extended with zero samples.)
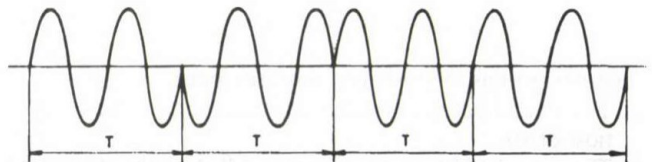- Computing the squared magnitude of the FFT spectrum.

Fig. 2. FFT based frequency detector (FFTFD)

The frequency where the squared magnitude spectrum has its maximum is considered as an instantaneous estimate of the carrier frequency.

However, the instantaneous frequency estimates fluctuate around a mean value, so we have to perform averaging. This is carried out by a filter referred to as "Avg. filter" in the following.

3. APPLICATION OF THE FFT FREQUENCY DETECTOR IN CARRIER SYNCHRONIZATION

The carrier synchronizer using the FFT frequency detector (FFTFD) is depicted in Fig. 3. Note that the FFTFD operates in a feed-forward structure. The PD is a sign type FDFL frequently used in many applications. (For simplicity, only the logic circuit is labeled as FDFL instead of the whole loop in Fig. 3.) The role of the signal sw will be explained later.
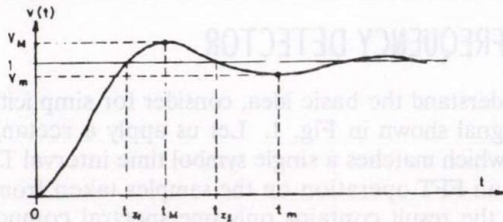

Fig. 3. FFTFD based carrier synchronizer

A further problem of the algorithm is that the expected value of the estimate is not exactly equal to the carrier frequency. Although this deviation compared with the frequency-offset is not too large $(6-7\%)$ [12], it can exceed the small lock-in range of the FDFL. The solution to this problem is to use some form of frequency sweeping techniques.

3.1. Sweeping by means of Avg. filter

If the Avg. filter has a pair of complex conjugate poles then the step response of the filter overshoots and rings around the steady state value. Hence the output of the second-order filter sweeps through the desired VCO control signal range within which the FDFL could lock in.

Consider a pair of complex conjugate poles on the analog complex frequency plane shown in Fig. 4. The sampled version of the designed analog filter can be realized by means of the impulse-invariant transformation [9].
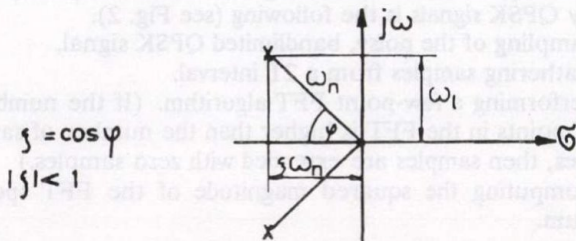
Fig. 4. Complex conjugate poles

The design has to satisfy two requirements:
1) The overshoot has to reach the maximum of the estimation error.
2) The speed of frequency sweeping ($\frac{d}{dt}\Delta\omega$) should not be greater than a given value because if the sweep speed exceeds this limit, the loop will be unable to acquire lock. The sweep speed is determined by the following inequality taken from [2] and including both theoretical and experimental contributions.

$$\frac{d}{dt}\Delta\omega < \frac{1}{2}\omega_{nL}^2 \left(1 - 2(SNR)_L^{-\frac{1}{2}} \right) \quad (1)$$

where ω_{nL} and $(SNR)_L$ are the natural frequency of

the FDFL and the loop signal-to-noise ratio [2], respectively.

The first requirement will be satisfied by setting the overshoot of the step response $v(t)$ shown in Fig. 5. Note that $\Delta\omega$ is proportional to $v(t)$. Assuming that the maximum estimation error V_M is known, ξ can be determined [10].
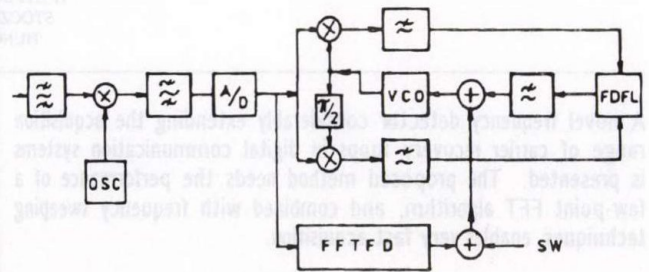
Fig. 5. Step response

The second requirement sets the upper limit of the step response slope. Since we want to choose the lock-in in the vicinity of t_{z1} (see Fig. 5), we have to find the time instant at which the slope has its first maximum value. If t_{mo} denotes the time instants where the slope of $v(t)$ has its first local maximum then for $\xi > 0.5$, $t_{z1}/t_{mo} > 2$ [10], [12]. So the maximum slope is far from the vicinity of the lock-in. Hence we can specify the sweep speed given in (1) at t_{z1}:

$$\frac{d}{dt}v(t_{z1}) < L(E_b/N_0) \quad (2)$$

where

$$L(E_b/N_0) = \frac{1}{K_0}\frac{1}{2}\omega_{nL}^2 \left(1 - 2(SNR)_L^{\frac{1}{2}} \right),$$

and K_0 is the VCO gain. Note that $(SNR)_L$ depends on E_b/N_0 and $\frac{d}{dt}v$ is the impulse response of the filter. Substituting ξ, the impulse response at t_{z1} [10] is

$$\frac{d}{dt}v(t_{z1}, \xi) = C_1\omega_n,$$

where C_1 is constant. Considering (2), the average lock-in time is $t_{z1} = C_2/\omega_n$, where C_2 is constant.

Taking $\omega_{nL} = 2\pi 471$ [r/s] and $K_0 = 512$ [kr/s/V] which seemed to be proper parameters in an earlier study [11], the results are shown in Table 1. The last column contains the lock-in times obtained by simulation which are gerater than the theoretical ones. According to the investigations, this fact is due to the pattern jitter not considered in (1).

Table 1. Average lock-in times in case of sweep using Avg. filter

E_b/N_0 [dB]	$L(E_b/N_0)$	ω_n [r/s]	t_{z1} [s]	t_{z1} [symbol]	t_{z1} [symbol] (simulation)
∞	8.55	58.58	0.05	1626	21140
9	7.21	49.42	0.06	1928	30850
6	6.65	45.59	0.07	2090	48000

3.2. Additional linear sweeping

In this method we add a linearly increasing sweep signal to the control signal coming from the FFTFD (see Figs. 2 and 6). Sweeping starts when Avg. filter reaches its steady state. The requirements for designing the sweep signal are similar to those applied previously for the step response.
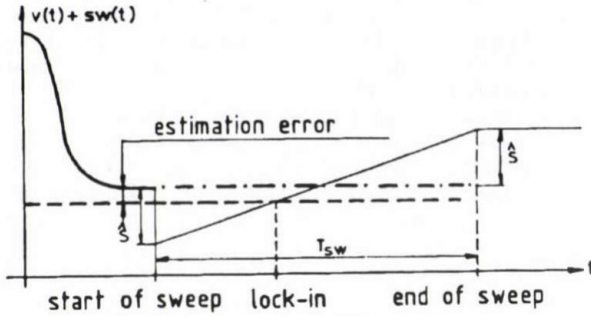

Fig. 6. Linearly swept VCO control signal

The general form of the sweep signal according to Fig. 6 is given by

$$sw(t) = \frac{2\hat{s}}{T_{sw}} t - \hat{s}$$

If the maximum estimation error is known then $\hat{s}$ is determined.

The slope of the straight line has to fulfil the inequality

$$\frac{d}{dt} sw = \frac{2\hat{s}}{T_{sw}} < L(E_b/N_0)$$

(The definition of $L(E_b/N_0)$ is given above.) Hence the lower limit of maximum sweep time is given by

$$T_{sw} > \frac{2\hat{s}}{L(E_b/N_0)}$$

Table 2. Average lock-in times in case of linear sweep

E_b/N_0 [dB]	$L(E_b/N_0)$	$T_{sw}/2$ [symbol]	$T_{sw}/2$ [symbol] (simulation)
∞	8.55	66	900
9	7.21	78	1250
6	6.65	84	2000

The theoretical and the simulated values of T_{sw} are different (see Table 2, $\omega_{nL} = 2\pi\ 471$ [r/s]) which can be explained by the presence of pattern jitter as mentioned above. The average lock-in time is half of T_{sw}. The computer simulation results for lock-in processes are shown in Fig. 7 for a noiseless channel and for $E_b/N_0 = 6$ dB.

The lock-in time of the FFT based synchronizer with linear sweeping takes about 700 symbols, and not more than 1500 symbols in the presence of channel noise as shown in Fig. 7.
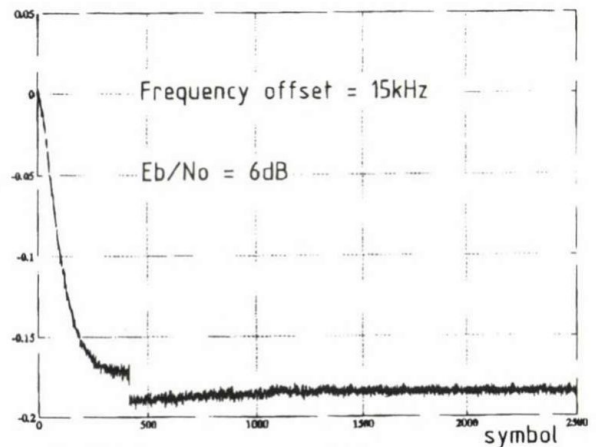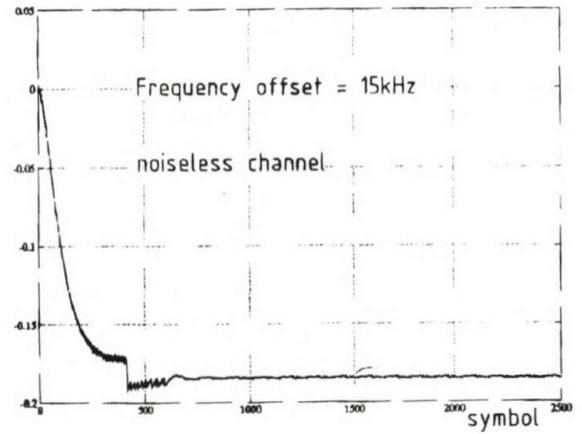
Fig. 7. VCO control signal in FFT based synchronizer

Although the common specification for the lock-in time in continuous-mode satellite modems corresponds to many thousands of symbols [7], the results obtained by using the Avg. filter for sweeping are unsatisfactory in practice. Much better performance can be achieved by linear sweeping.

4. CONCLUSIONS

We have presented a new FFT based method for fast carrier recovery in digital communication systems. The proposed algorithm is particularly applicable in continuous-mode QPSK satellite modems where the signal to noise ratio is rather low and the carrier frequency-offset is large. We have developed a frequency detector based on FFT and operating in a carrier recovery circuit together with a simple conventional PD. The lock-in process of the PD is aided efficiently by a linear sweeping technique since the new FD produces a distorted frequency estimation. The performance of the new carrier recovery circuit was tested by means of computer simulation. The results show that the new FFT frequency detector yields an acquisition time which is shorter than that of the conventional carrier recovery circuits [12], [13].

5. ACKNOWLEDGEMENT

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DOES LOW COMPLEXITY PRECLUDE HIGH SPEECH QUALITY IN THE RPE-GSM SPEECH CODEC?

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In the freshly standardised Pan-European GSM mobile radio system, uncompromised speech quality, high bandwidth efficiency and robustness are required. Subband codes (SBC) and multi-pulse excited (MPE) or regular pulse excited (RPE) codecs are potentially well suited, with the SBC having slightly lower complexity and speech quality than the pulse excited codecs. With the proviso of powerful DSP chips, the complexity advantage of SBCs is diminishing, particularly if the pulse excited codecs can be 'tamed' in terms of complexity while maintaining high speech quality. The best compromise between quality and complexity at today's technology is represented by the RPE codec. It is shown that the notorious matrix inversion in the excitation optimisation of the RPE codec is eliminated at virtually no cost in speech quality, resulting in dramatic complexity reduction. The simulated GSM-standardised codec has a bitrate of 13 kbps, mean opinion score (MOS) of 4 and segmental signal-to-noise ratio (SEGSNR) around 15 dB, while maintaining high robustness against channel errors.

1. INTRODUCTION

After nearly a decade of research and development (R&D), 12 European countries have finalised the recommendations for the digital Pan-European mobile radio system referred to as GSM (Group Speciale Mobile), and the system's launch is planned for 1992. The system has been designed to be superior to any of the existing analog mobile networks in terms of almost all specifications, which imposes nearly unsurmountable difficulties on the chip designers as regards to packaging densities and power consumption.

In this contribution, we focus our attention on pure speech coding aspects, and after a brief historic overview of the 1988 Paris speech codec 'beauty contest', where the 13 kbps GSM regular pulse excited (RPE) speech codec was 'crowned', we demonstrate how the problem of high computational complexity can be circumvented while maintaining high speech quality. Our arguments and results are justified and supported by simulation results [1], [10].

2. CANDIDATE CODECS AND THEIR COMPARISON

Originally, the participating countries have proposed six different codecs for comparison. At a preliminary test the codecs were compared to the presently used companded FM system, and then two of the codecs were withdrawn.

The remaining codecs were two different subband codecs and two pulse-excited codecs, as detailed below:

1. *SBC-APCM:* Subband codec with block adaptive PCM

This codec used quadrature mirror filters (QMF) to split the input signal into 16 subbands of bandwidth 250 Hz, out of which the two highest bands were not transmitted. Adaptive bit allocation was used in the subbands on the basis of the power ratios of the various subbands, which constituted the side-information to be transmitted. The gross transmission rate of the subband signals was 10 kbit/s and the side-information was 3 kbit/s.

2. *SBC-ADPCM:* Subband codec with adaptive delta PCM

In this scheme, the speech input signal was split into 8 subbands, but only 6 were transmitted. The subband signals were encoded by differential PCM coding with backward estimation and adaptation, as opposed to the SBC-APCM candidate where forward estimation and adaptation was used. The bit allocation over the subbands was fixed, hence no side-information was transmitted which made the scheme more noise resilient and the bitrate was 15 kbits/s only.

3. *MPE-LTP:* 13.2 kbps multi-pulse excited LPC codec with long-term predictor

4. *RPE-LPC:* 13 kbps regular pulse excited LPC codec

These four codecs were compared in terms of speech quality, robustness, processing delays and computational complexity. From the experience with the companded FM reference system two benchmarker bit error ratios (BER) were supposed, at which performance comparisons were carried out. The pessimistic case was a $BER = 10^{-2} = 1\%$, which would incur a carrier to noise ratio (CNR) of approx. 18 dB, exceeded probably in 90% of the reception area. The optimistic channel exhibits a $BER = 10^{-3} = 0.1\%$, requiring approx. $CNR = 26$ dB, guaranteed for at least 50% of the coverage area for the reference FM system.

The average mean opinion scores (MOS) on a five point scale over a range of test conditions were found to be:

MOS (RPE-LPC) = 3.54
MOS (MPE-LTP) = 3.27
MOS (SBC-APCM) = 3.14
MOS (SBC-ADPCM) = 2.92
MOS (FM) = 1.95

A variety of SBC codecs are published in [1], [12] and [13], the MPE principle is introduced in [2], while this

contribution is devoted to the description of the improved RPE-LTP codec. Clearly, all codecs, outperformed the analog system by a definite margin. Also, the longstanding battle of the lower complexity open-loop SBC codecs and higher complexity analysis-by-synthesis pulse excited codecs seems to have come to an end with the diminishing importance of the lower complexity of SBCs, if power consumption is not a prime issue. Lastly, the importance of the additional LTP used in the MPE codec was duly recognised by the GSM expert group, and a decision was taken to introduce an LTP in the RPE codec which was an outright winner even without LTP. Let us therefore now concentrate on the improved winner, the RPE-LTP codec.

3. DERIVATION OF TH RPE KEY-EQUATION

The general structure of analysis-by-synthesis codecs is shown in Figure 1, where the excitation vectors $v(n)$ $\{n = 1 \ldots N\}$ (typically $n = 40$) are filtered through the long-term predictor (LTP) synthesis filter $1/P(z)$ to model the short-term prediction (STP) residual $r(n)$ by the signal $u(n)$. The signal $u(n)$ is then convolved with the impulse response $h_w(n)$ of the cascaded filter complex constituted by the STP synthesis filter $1/A(z)$ and the perceptual error weighting filter $W_1(z) = A(z)/A(z/\gamma)$ to produce the weighted synthetic speech $\hat{s}_{w_1}(n)$. Observe that

$$1/A(z) \times A(z)/A(z/\gamma) = 1/A(z/\gamma) = W(z)$$

is a simplified version of the weighting filter $W_1(z)$ which is used throughout our further discourse. Then the weighted error is given by

$$e_w(n) = s_w(n) - \hat{s}_w(n), \quad (1)$$

where the weighted synthetic speech is computed as

$$\hat{s}_w(n) = v(n) * h_p(n) * h_w(n) = v(n) * h_c(n) \quad (2)$$

with $h_p(n)$ being the LTP synthesis filter's impulse response, while $h_c(n) = h_p(n) * h_w(n)$ is that of the filter complex $W(z)/P(z)$.

To achieve good perceptual speech quality it is crucial to recognize that the filters $h_p(n)$, $h_w(n)$ and $h_c(n)$ have a memory of p samples. This memory has to be carried across the speech frame boundaries from the previous frame when computing the first p samples of the present frame. In practical terms we are faced with the problem of inputting all legitimate excitation sequences to the synthesis filter $h_c(n)$ and finding that specific one which minimises the weighted error $e_w(n)$ over a frame of usually $N = 40$ samples, i.e. over a subsegment of 5 ms. When substituting each synthetic speech frame given by Eq(2) into Eq(1), the memory of $h_c(n)$ in response to the previous optimum excitation has to be subtracted from $\hat{s}_w(n)$. This memory contribution is saved in a temporary buffer, subtracted from $\hat{s}_w(n)$, and finally the memory of $h_c(n)$ must be reset to zero before the new excitation vectors are inputted to it to compute $\hat{s}_w(n)$.

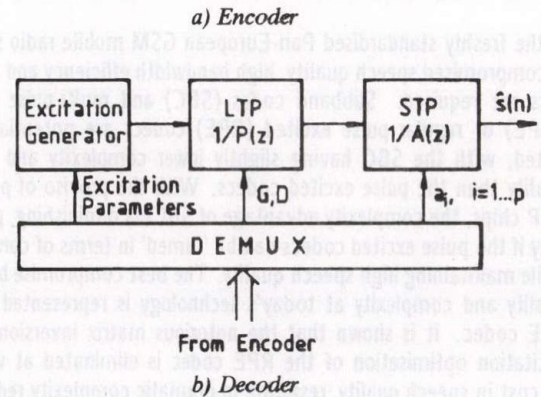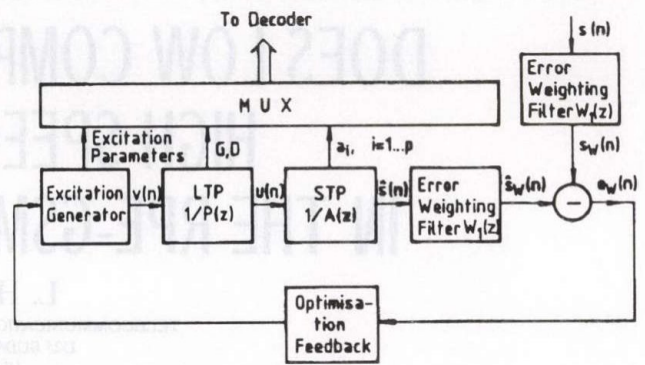*a) Encoder*

b) Decoder

Fig. 1. Time-domain hybrid codec with LTP

The mathematics is detailed in [1] and [14], here we simply rephrase Eq(1) as

$$e_w(n) = \hat{s}_w(n) - s_{mem}(n) - v(n) * h_c(n) = \\ = x(n) - v(n) * h_c(n), \quad (3)$$

where $x(n)$ is the weighted original speech after removing the memory of $h_c(n)$ inherited from the previous frame. The RPE excitation vector $v(n)$ is assumed to hold M number of equidistant excitation samples with amplitudes β_k and positions m_k, and thence

$$v(n) = \sum_{k=1}^{M} \beta_k \delta(n - m_k), \quad (4)$$

yielding

$$e_w(n) = x(n) - \sum_{k=1}^{M} \beta_k h_c(n - m_k). \quad (5)$$

The total mean squared error (mse) for a block of N speech samples is given by

$$E_w = \sum_{n=0}^{N-1} e_w^2(n) = \quad (6)$$

$$= \sum_{n=0}^{N-1} \left[x(n) - \sum_{k=1}^{M} \beta_k h_c(n - m_k) \right]^2.$$

By setting the partial derivatives of E_w in Eq(6) with respect to the pulse amplitudes β_i, $i = 1 \ldots M$ to zero, we get

$$\Psi(m_i) = \sum_{k=1}^{M} \beta_k \Phi(m_i, m_k) \quad \text{for} \quad i = 1 \ldots M, \quad (7)$$

where

$$\Psi(m_i) = x(n) * h_c(-n) \qquad (8)$$

is formally the weighted memoryless synthetic speech, and

$$\Phi(m_i, m_k) = \sum_{n=0}^{N-1} h_c(n - m_k) \times h_c(n - m_i) \qquad (9)$$

is the covariance of the impulse response $h_c(n)$. Portrayed in matrix form we have

$$
\begin{pmatrix}
\Phi(m_1, m_1) & \cdots & \Phi(m_1, m_M) \\
\Phi(m_2, m_1) & \cdots & \Phi(m_2, m_M) \\
\cdot & , & \cdot \\
\cdot & , & \cdot \\
\Phi(m_M, m_1) & \cdots & \Phi(m_M, m_M)
\end{pmatrix}
\begin{pmatrix}
\beta_1 \\ \beta_2 \\ \cdot \\ \cdot \\ \beta_M
\end{pmatrix} =
$$

$$
= \begin{pmatrix}
\Psi(m_1) \\ \Psi(m_2) \\ \cdot \\ \cdot \\ \Psi(m_M)
\end{pmatrix} \qquad (10)
$$

Eq(7) is a set of M linear equations that should be solved for M pulse amplitudes plus M pulse positions which is certainly unviable. A historically important suboptimum solution was suggested by Atal [2], which is the so-called multi-pulse excited (MPE) codec. Another attractive approach proposed by Kroon et al. [3] is the regular pulse excited (RPE) codec, which is going to be described next.

4. SOLVING THE RPE KEY-EQUATION

According to the RPE approach, the innovation sequence is derived as a subsampled version of the STP residual. The excitation pulses are d samples apart and there are d decimated candidate excitation sequences according to the d possible initial grid-positions. If a frame of N prediction residual samples is processed, the number of excitation pulses is given by $M = (N) \text{ Div } (d)$. The legitimate excitation pulse positions are

$$m[k, i] = k + (i - 1)d, \qquad i = 1, 2, \ldots M,$$

where

$$k = 0, 1, \ldots (d - 1)$$

are the initial grid-positions. With the pulse-positions fixed, the key-equation Eq(7) is solved d times for each candidate excitation pattern, yielding d sets of M pulse amplitudes.

Now the candidate innovation sequences are known, whence the mse E_w can be computed for all of the d sequences, and the one minimising the weighted mse E_w is elected as innovation sequence. Using Eq(5) E_w is yielded as:

$$E_w = \sum_{n=0}^{N-1} e_w^2(n) =$$

$$= \sum_{n=0}^{N-1} \left[x(n) - \sum_{k=1}^{M} \beta_k h_c(n - m_k) \right]^2, \qquad (11)$$

which can be simplified to

$$E_w = \sum_{n=0}^{N-1} x^2(n) - \sum_{k=1}^{M} \beta_k \Psi(m_k), \qquad (12)$$

where E_w is minimised if the second term of Eq(12) is maximised.

The key-equation Eq(10) can be solved either by matrix inversion using Gaussian elimination or deploying Cholesky-decomposition which has a complexity proportional to M^3. For the typical values of $N = 40$ and $d = 4$, $M = 10$ equations have to be solved four times during the 5 ms subsegment period. Besides, Eq(8) and Eq(9) have to be evaluated as well.

5. REDUCING THE RPE COMPUTATIONAL COMPLEXITY

The computational complexity incurred in solving Eq(10) is beyond the capacity of the fastest state-of-art DSP chip, hence we have to embark upon reducing the complexity while maintaining high speech quality. Significant simplification is achieved at almost imperceptible quality degradation by assuming that the speech is stationary, rendering the covariance $\Phi(i, j)$ to become $\Phi(|i - j|) = \Phi(k)$.

With this assumption, the key-equation Eq(10) is simplified to

$$
\begin{pmatrix}
\Phi(0) & \Phi(d) & \Phi(2d) & \cdots & \Phi((M-1)d) \\
\Phi(d) & \Phi(0) & \Phi(d) & \cdots & \Phi((M-2)d) \\
\cdot & \cdot & , & , & \cdot \\
\cdot & \cdot & , & , & \cdot \\
\Phi((M-1)d) & \cdots & & & \Phi(0)
\end{pmatrix} \times
$$

$$
\times \begin{pmatrix}
\beta(k, 1) \\ \beta(k, 2) \\ \cdot \\ \cdot \\ \beta(k, M)
\end{pmatrix} =
\begin{pmatrix}
\Psi(m(k, 1)) \\ \Psi(m(k, 2)) \\ \cdot \\ \cdot \\ \Psi(m(k, M))
\end{pmatrix} \qquad (13)
$$

where the correlation matrix Φ becomes Töplitz. For Töplitz-type systems, a plethora of computationally efficient iterative algorithms is available, amongst which the Levinson−Durbin, Robinson, Berlekamp−Massey, Schur and Burg algorithms are best known, all exhibiting a complexity proportional to M^2 rather than M^3.

Further dramatic complexity reduction accrues if the correlation matrix Φ is arranged to be that of a time-invariant weighting filter $h_c(n)$. Clearly, rather than using the time-variant LPC coefficients a_k, $k = 1 \ldots p$, the long-term average correlation coefficients are deployed in $h_c(n) = z\{W(z)\}$ where

$$W(z) = \frac{1}{C(z/\gamma)} = \frac{1}{1 - \sum_{k=1}^{K} c_k \gamma^k z^{-k}}. \qquad (14)$$

A set of fixed long-term correlation coefficients derived by Flanagan et al. [4] for a sampling frequency of 8 kHz is $r_0 = 1$, $r_1 = 0.85$, $r_2 = 0.562$, $r_3 = 0.308$. A simple

fixed third order predictor derived from these correlations and successfully utilised in DPCM systems is given by $c_0 = 1.1$, $c_1 = -0.28$, $c_2 = -0.08$. Then with a typical value of $\gamma \approx 0.8$, we have

$$h_c(n) = \sum_{k=0}^{2} c_k \gamma^k h_c(n-k), \quad n = 0 \ldots N-1 \quad (15)$$

and

$$\Phi(i) = \sum_{n=i}^{N-1} h_c(n)h_c(n-i). \quad (16)$$

As we have seen, $h_c(n)$ is a sharply decaying function, therefore $\Phi(i)$ decays even faster. This allows us to set all off-diagonal elements in the covariance matrix Phi to zero, resulting in tremendously reduced complexity when solving the key-equation Eq(10) as evidenced by

$$\Phi(0) \begin{pmatrix} \beta & (k,1) \\ \beta & (k,2) \\ \cdot \\ \cdot \\ \cdot \\ \beta & (k,M) \end{pmatrix} = \begin{pmatrix} \Psi & (m(k,1)) \\ \Psi & (m(k,2)) \\ \cdot \\ \cdot \\ \cdot \\ \Psi & (m(k,M)) \end{pmatrix} \quad (17)$$

$$\beta(k,i) = \frac{\Psi[m(k,i)]}{\Phi(0)}. \quad (18)$$

Neglecting the weighting filter's memory enables us to compute $\Phi(m_i)$ in Eq(8) as

$$\Phi(n) = x(n) * h_c(-n) = s_w(n) * h_c(-n) =$$
$$= r(n) * h_w(n) * h_c(-n). \quad (19)$$

If the minimum LTP delay is restricted to $D > N = 40$, then the LTP does not influence the impulse response $h_c(n)$ for values of $n < N = 40$ and therefore $h_w(n) = h_c(n)$, yielding

$$\Psi(n) = r(n) * h_c(n) * h_c(-n) = r(n) * \Phi(n). \quad (20)$$

Substituting $\Psi(m_i)$ from Eq(20) into Eq(18) gives

$$\beta(k,i) = r[m(k,i)] * \frac{\Phi[m(k,i)]}{\Phi(0)} =$$
$$= r[m(k,i)] * \phi[m(k,i)], \quad (21)$$

where the normalised autocorrelation $\phi[m(k,i)]$ of the impulse response represents a fixed, symmetric smoother or low-pass filter (LPF). For a pulse-spacing of $d = 3$, as in the GSM-standard RPE codec [5], a cutoff frequency of $f_c = 1.3$ kHz has to be used. For an ideal 'rectangular' low-pass FIR-filter of order 11, the symmetric impulse re-

sponse coefficients are simply derived from the Hamming-windowed sinc function:

$$\begin{aligned}
\phi(0) &= \phi(10) = -0.016256 \\
\phi(1) &= \phi(9) = -0.045649 \\
\phi(2) &= \phi(8) = 0 \\
\phi(3) &= \phi(7) = 0.250793 \\
\phi(4) &= \phi(6) = 0.70079 \\
\phi(5) &= 1
\end{aligned} \quad (22)$$

Having determined the pulse amplitudes in Eq(18), the minimum weighted mse E_w^j of each candidate excitation vector is computed as

$$E_w^{(j)} = \sum_{n=0}^{N-1} s_w^2(n) - \Phi(0) \sum_{k=1}^{M} \beta^2(k,i) =$$
$$= \sum_{n=0}^{N-1} s_w^2(n) - \Phi(0)E(j), \quad (23)$$

where $E(j)$ is the energy of the j-th candidate excitation vector. It becomes plausible now that the specific excitation vector having the highest energy minimises E_w. This is in harmony with our expectations, since this very vector gives the best representation of the prediction residual $r(n)$ when generating the synthetic speech.

Our previous discourse culminates here in the summary of the simplified RPE algorithm as follows:

1. The STP residual $r(n)$ is convolved with the LPF impulse response $\phi(n)$ specified in Eq(22), where only the N central samples are retained.
2. The result is decomposed into $d = 3$ candidate sequence and their energies are computed.
3. The error E_w is minimised by the sequence exhibiting the highes energy, therefore this innovation sequence is coded for transmission to be used at the decoder in producing the synthetic speech.

Bearing in mind the RPE error minimisation algorithm highlighted, let us now embark upon the description of the RPE codec.

6. THE RPE-LTP ENCODER

The schematic diagram of the RPE-LTP encoder is shown in Figure 2 where the following functional parts can be recognised [6], [7]:
1. Pre-processing
2. STP analysis filtering
3. LTP analysis filtering
4. RPE computation

Pre-processing

Pre-emphasis is deployed to increase the numerical precision in computations by emphasizing the high-frequency, low-power part of the speech spectrum. This can be carried out by the help of a one-pole filter with the transfer function of

$$H(z) = 1 - c_1 z^{-1}, \quad (24)$$

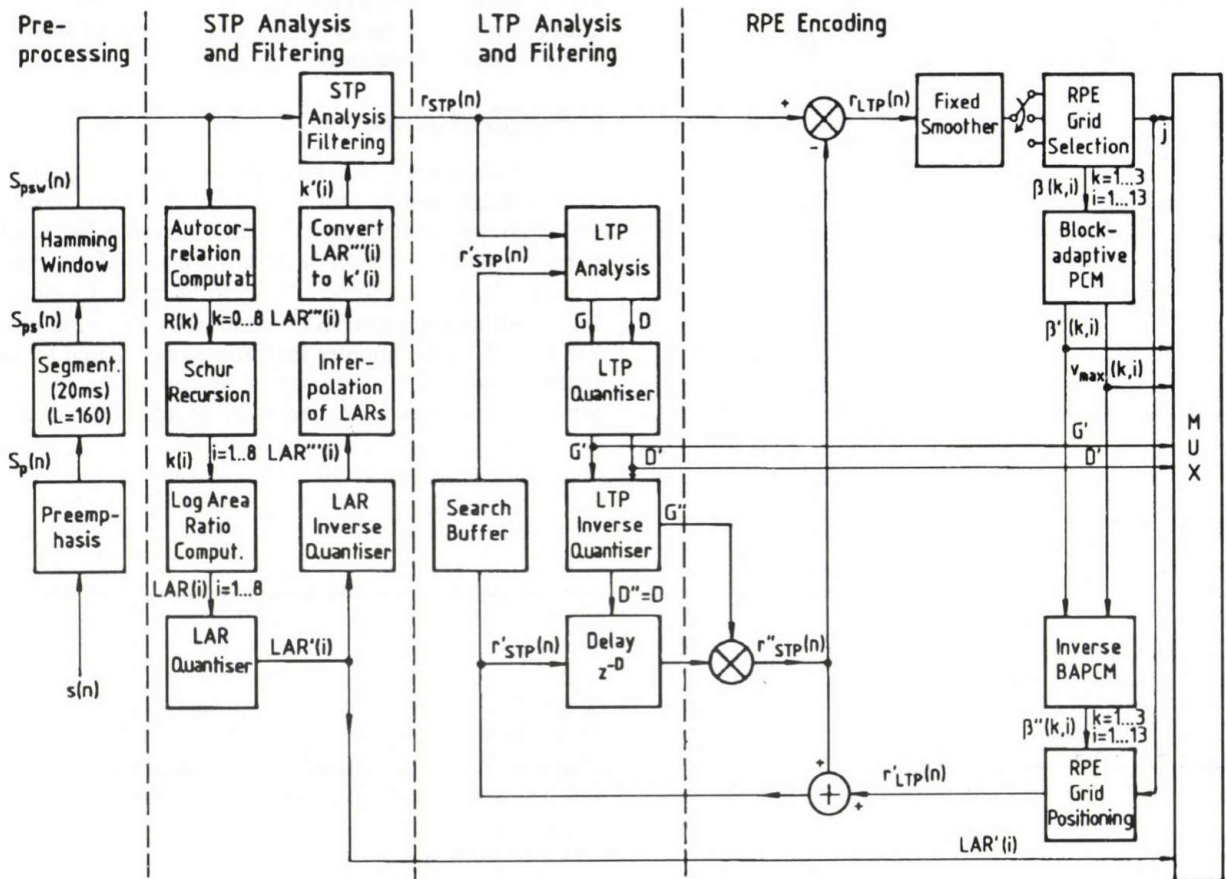where $c_1 \sim 0.9$ is a practical value.

Figure 2. Block diagram of the RPE-LTP encoder

The pre-emphasized speech $s_p(n)$ is segmented into blocks of $L = 160$ samples in a buffer, where they are Hamming-windowed to counteract the spectral domain Gibbs oscillation caused by truncating the speech signal outside the analysis frame. The Hamming-window has a tapering effect towards the edges of a block, while it has no influence in its middle ranges:

$$s_{psw}(n) = s_{ps}(n) \times c_2 \times \left(0.54 - 0.46 \cos 2\pi \frac{n}{L}\right), \quad (25)$$

where $s_{ps}(n)$ represents the pre-emphasized segmented speech, $s_{psw}(n)$ is its windowed version and the constant $c_2 = 1.5863$ is determined from the condition that the windowed speech must have the same power as the non-windowed.

STP analysis filtering

For each segment of $L = 160$ samples, nine autocorrelation coefficients $R(k)$ are computed from $s_{psw}(n)$ by

$$R(k) = \sum_{n=0}^{L-1-k} s(k)s(n+k); \quad k = 0\ldots8. \quad (26)$$

From the speech autocorrelations $R(k)$ eight reflection coefficients k_i are computed according to the Schur-recursion [8] which is an equivalent method to the Durbin

algorithm used for solving the LPC key-equations to derive the reflection coefficients $k(i)$ as well as the STP filter co-efficients $a(i)$. However, the Schur-recursion delivers the reflection coefficients $k(i)$ only. The reflection coefficients $k(i)$ are converted to logarithmic area ratios (LAR(i)), because the logarithmically companded LARs have a near-uniform probability density and hence better quantisation properties than the coefficients $k(i)$:

$$LAR(i) = \log_{10}\left(\frac{1 + k(i)}{1 - k(i)}\right), \quad (27)$$

where a piecewise linear approximation with five segments is used to simplify the real-time implementation:

$$LAR'(i) = k(i),$$
if $|k(i)| < 0.675$
$$LAR'(i) = \text{sign}\,[k(i)][2 \times |k(i)| - 0.675],$$
if $0.675 < |k(i)| < 0.95$ \quad (28)
$$LAR'(i) = \text{sign}\,[k(i)][8 \times |k(i)| - 6.375],$$
if $0.975 < |k(i)| < 1.0$

The various LAR(i) $= 1\ldots8$ filter parameters have different dynamic ranges and differently shaped probability density functions (PDFs) as seen in Figure 3. This justifies the allocation of 6,5, 4 and 3 bits to the first, second, third and fourth pairs of LARs, respectively.
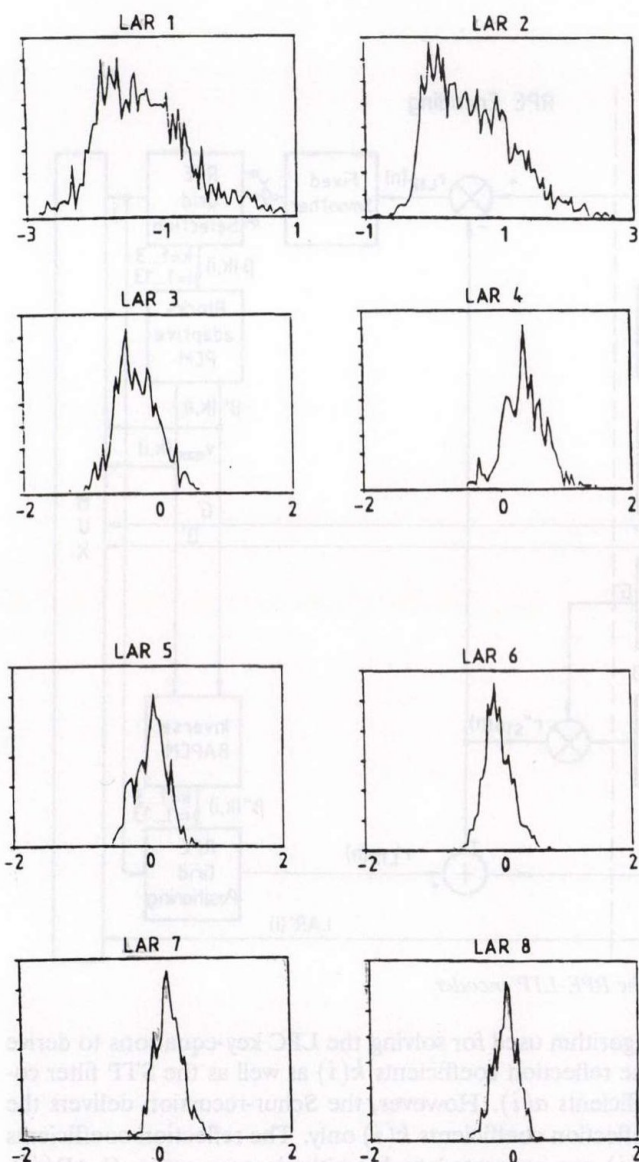
31

Figure 3. PDFs of LAR filter parameters
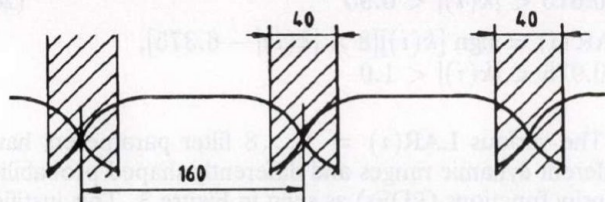
STP residual $r_{STP}(n)$ in a PARCOR structure [9]. The PARCOR scheme directly uses the reflection coefficients $k(i)$ to compute the STP residual $r_{STP}(n)$, and it constitutes the natural analogy to the acoustic tube model of the human speech production.

LTP analysis filtering

When computing the LTP parameters, the prediction error is minimised by that LTP delay D which maximises the crosscorrelation between the current STP residual $r_{STP}(n)$ and its previously received and buffered history at delay D, i.e. $r_{STP}(n - D)$. To be more specific, the $L = 160$ samples long STP residual $r_{STP}(n)$ is divided into four $N = 40$ samples long subsegments, and for each of them, one LTP is determined by computing the crosscorrelation between the presently processed subsegment and a continuously sliding $N = 40$ samples long segment of the previously received 128 samples long STP residual segment $r_{STP}(n)$. The maximum of the correlation is found at a delay D where the currently processed subsegment is the most similar one to its previous history. This is most probably true at the pitch periodicity or at a multiple of the pitch periodicity. Hence the most redundancy can be extracted from the STP residual, if this highly correlated segment is substracted from it, multiplied by a gain factor G which is the normalised crosscorrelation found at delay D, as shown in Figure 5. Once the LTP filter parameters G and D have been found, they are quantised to give G' and D' where G is quantised only by two bits, while to quantise D' seven bits are sufficient.
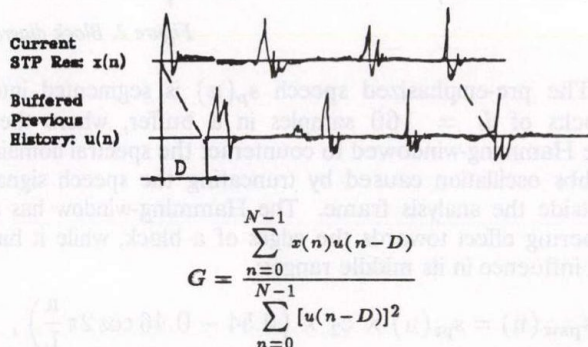

$$G = \frac{\sum_{n=0}^{N-1} x(n)u(n-D)}{\sum_{n=0}^{N-1} [u(n-D)]^2}$$

Figure 5. LTP analysis filtering

The quantised LTP parameters (G', D') are locally decoded into the pair (G'', D'') so as to produce the locally decoded STP residual $r'_{STP}(n)$ for use in the forthcoming subsegments to provide the previous history of the STP residual for the search buffer, as shown in Figure 2.

With the LTP parameters just computed, the LTP residual $r_{LTP}(n)$ is calculated as the difference of the STP residual $r_{STP}(n)$ and its estimate $r''_{STP}(n)$ which has been computed by the help of the locally decoded LTP parameters (G'', D) as shown below:

$$r_{LTP}(n) = r_{STP}(n) - r''_{STP}(n), \quad (29)$$

$$r''_{STP}(n) = G'' \times r'_{STP}(n - D). \quad (30)$$

Here $r'_{STP}(n - D)$ represents an already known segment of the past history of $r'_{STP}(n)$, stored in the search buffer. Finally, the content of the search buffer is updated by us-

The quantised LAR(i) coefficients LAR'(i) are locally decoded into the set LAR"(i) as well as transmitted to the speech decoder. So as to mitigate the abrupt changes in the nature of the speech signal envelope due to switching the set of LARs at the STP analysis frame edges, the LAR parameters are linearly interpolated between adjacent LPC analysis frames, and towards the edges of an analysis frame, the interpolated LAR'"(i) parameters are used, as shown in Figure 4. Now the locally decoded reflection coefficients $k'(i)$ are computed by converting LAR'"(i) back into $k'(i)$ which are used to compute the

Figure 4. Interpolation of LARs

ing the locally decoded LTP residual $r'_{\text{LTP}}(n)$ and the estimated STP residual $r''_{\text{STP}}(n)$ to form $r'_{\text{STP}}(n)$, as shown below:

$$r'_{\text{STP}}(n) = r'_{\text{LTP}}(n) + r''_{\text{STP}}(n). \tag{31}$$
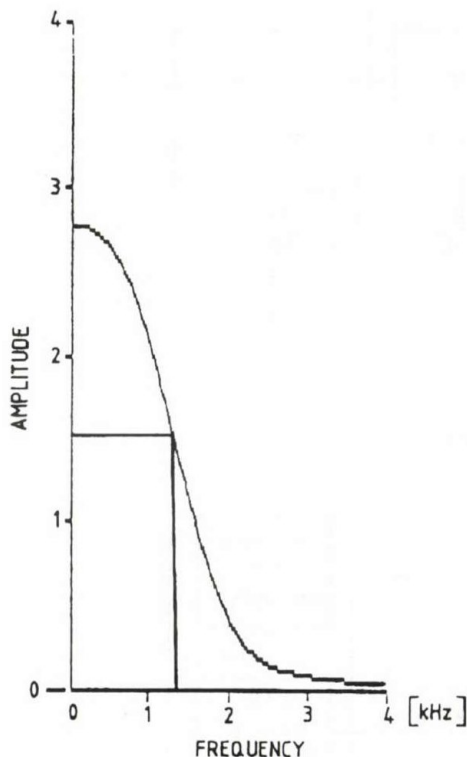

Figure 6. Magnitude versus frequency for the fixed smoother

RPE coding

The LTP residual $r_{\text{LTP}}(n)$ is weighted with the fixed error weighting smoother, as shown in Figure 2. The impulse response of the fixed smoother can be derived from the long-term speech autocorrelation coefficients given in [4]. The frequency response of it has a gracefully decaying low-pass characteristic, as shown in Figure 6. For an RPE spacing or decimation factor of $d = 3$ proposed, the 3 dB cutoff frequency f_c has to be at $f_c = f_s/2d = 8000\ \text{Hz}/6 = 1.33$ kHz as seen in Figure 6, where $f_s = 8000$ Hz is the sampling frequency. The smoothed LTP residual $r_{\text{SLTP}}(n)$ is then decomposed into three excitation candidates, as displayed in Figure 7. The 40th sample of each $N = 40$ long subsegment is actually discarded, since the three candidate sequences can host 39 samples only. Then the energies E_1, E_2 and E_3 of the three decimated, 13 samples long candidate sequences are computed, and the candidate with the highest energy is chosen to be the best representation of the LTP residuals. The excitation pulses are afterwards normalised to the highest amplitude $v_{\text{max}}(k, i)$ in the sequence of the 13 samples, and they are quantised by a three bit uniform quantiser, whereas the logarithm of the block maximum $v_{\text{max}}(k, i)$ is quantised with six bits. According to three possible initial grid positions j, two bits are needed to encode the initial offset of the grid for each subsegment.
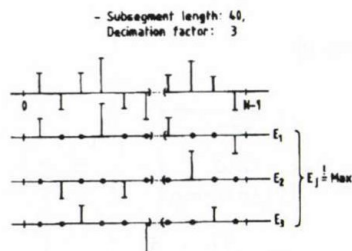
Figure 7. Innovation sequence computation

The pulse amplitudes $\beta(k, i)$, the grid positions j and the block maxima $v_{\text{max}}(k, i)$ are locally decoded to derive the LTP residual $r'_{\text{LTP}}(n)$, where the 'missing pulses' in the sequence are filled with zeros.
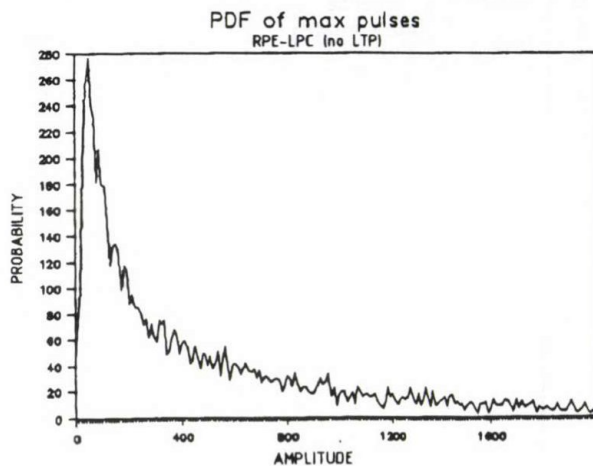

Figure 8. PDF of the excitation maximum pulses

To justify the quantisation schemes proposed, the probability density function(PDF) of the maximum excitation pulses has been evaluated and depicted in Figure 8. The exponential decay of the curve suggests that a logarithmic quantiser would flatten its sharply falling slope and result in more efficient quantisation. Then a near-uniform distribution is reached which can judiciosly be quantised by a uniform quantiser. The PDF of the normalised excitation pulses is shown in Figure 9. Since the distribution is relatively flat, a uniform quantiser guarantees low quantisation error variance. However, we have achieved better results by deploying a three-bit Max-Lloyd quantiser [10].
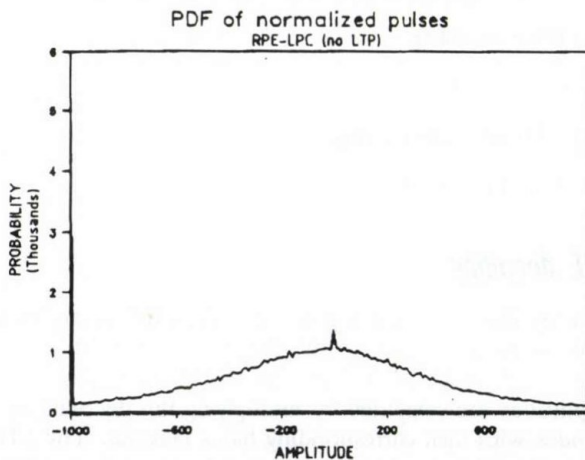

Figure 9. PDF of the normalised excitation pulses
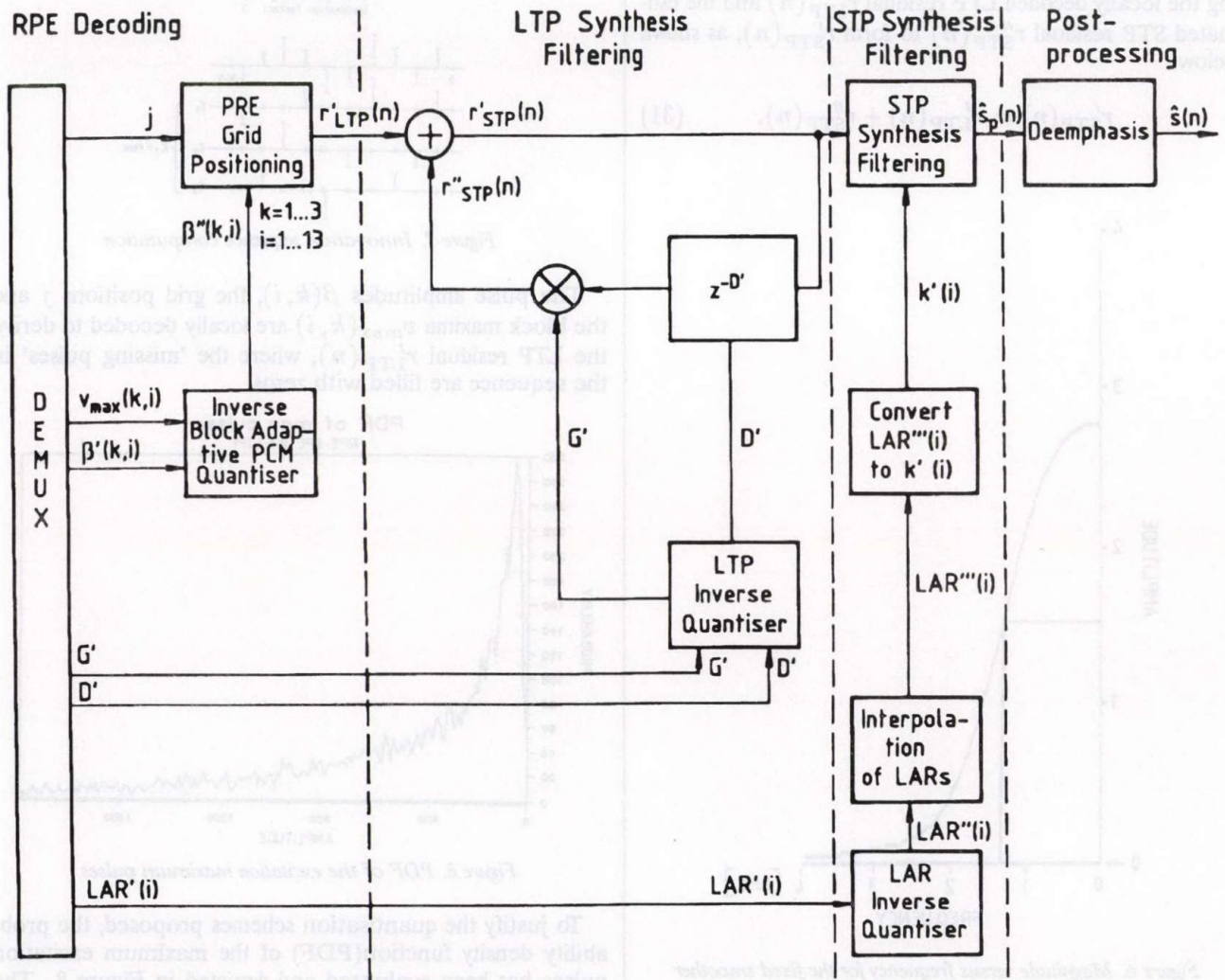

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Figure 10. Block diagram of the RPE-LTP decoder

7. THE RPE-LTP DECODER

The block diagram of the RPE-LTP decoder is shown in Figure 10 which exhibits an inverse functional structure to that of the encoder, depicted in Figure 2, namely:

1) RPE decoding

2) LTP synthesis filtering

3) STP synthesis filtering

4) Post-processing

RPE decoding

In the decoder, the grid position j, the subsegment excitation maxima $v_{max}(k,i)$ and the excitation pulse amplitudes $\beta'(k,i)$ are inverse quantised, and the actual pulse amplitudes are computed by multiplying the decoded amplitudes with their corresponding block maxima. The LTP residual model $r'_{LTP}(n)$ is recovered by properly positioning the pulse amplitudes $\beta(k,i)$ according to the initial offset j.

LTP synthesis filtering

Firstly the LTP filter parameters (G', D') are inverse quantised to derive the LTP synthesis filter. Then the recovered LTP excitation model $r'_{LTP}(n)$ is used to excite this LTP synthesis filter (G', D') to recover a new subsegment of length $N = 40$ of the estimated STP residual $r'_{STP}(n)$. To do so, the past history of the recovered STP residual $r'_{STP}(n)$ is used, properly delayed by D' samples and multiplied by G' to deliver the estimated STP residual $r''_{STP}(n)$, according

$$r''_{STP}(n) = G' \times r'_{STP}(n - D'), \quad (32)$$

and then $r''_{STP}(n)$ is used to compute the most recent subsegment of the recovered STP residual, as given below:

$$r'_{STP}(n) = r''_{STP}(n) + r'_{LTP}(n). \quad (33)$$

LAR No.	Minimum	Maximum	Stepsize	Bit No.
1	−2.3	0.9	0.05	6
2	−0.7	2.5	0.05	6
3	−1.0	0.6	0.05	5
4	−0.55	1.05	0.05	5
5−6	−0.8	0.8	0.1	4
7−8	−0.4	0.4	0.1	3
Total				36

STP synthesis filtering

To compute the synthesized speech $\hat{s}(n)$, the PARCOR synthesis is used [9] where similarly to the STP analysis, filtering the reflection coefficients $k(i)$ $i = 1 \ldots 8$ are required. The LAR'(i) parameters are decoded by using the LAR inverse quantiser to give LAR"(i), which are again linearly interpolated towards the analysis frame edges, between parameters of the adjacent frames, to prevent abrupt changes in the character of the speech spectral envelope, as suggested by Figure 4. Finally, the interpolated parameter set is transformed back into reflection coefficients where filter stability is guaranteed if recovered reflection coefficients, which fell outside the unit circle are reflected back into it by taking their reciprocal values. The inverse formula to convert LAR(i) back into $k(i)$ is given by:

$$k(i) = \frac{10^{\text{LAR}(i)} - 1}{10^{\text{LAR}(i)} + 1}. \qquad (34)$$

Post-processing

The post-processing is constituted by the de-emphasis, using the inverse filter of Eq(24), as given below:

$$H(z) = 1 + c_1 z^{-1}. \qquad (35)$$

In summary of the RPE-LTP encoding method, we tabulate the bit allocation scheme in Table 2 for a period of 20 ms, which is equivalent to the encoding of $L = 160$ samples.

Table 2. Bit-allocation scheme of the RPE-LTP codec

Parameter to be encoded	No. of bits
8 STP LAR coefficients	36 (see Table 7.3.2)
4 LTP Gains G	$4 \times 2 = 8$
4 LTP Delays D	$4 \times 7 = 28$
4 RPE Grid-positions	$4 \times 2 = 8$
4 RPE Block maxima	$4 \times 6 = 24$
$4 \times 13 = 52$ Pulse amplitudes	$52 \times 3 = 156$
Total bitnumber per 20 ms	260
Transmission bitrate	13 kbit/s

RPE codec evaluation by simulation

An approximately 40 ms segment of voiced speech generated by the simulated RPE-LPC codec is shown in Fig-

ure 11 along with the corresponding LPC residual and the regular pulse excitation computed. The segmental SNR (SEG-SNR) variation of the codec is displayed as an objective quality measure in Figure 12 vs. time, when the sentence "To reach the end he needs much courage" is uttered by a female speaker. The speech signal's waveform is also shown in Figure 12. The SEG-SNR is quite high in high energy voiced speech segments, while it becomes even negative sometimes in unvoiced or silent periods. There is a 25 dB SEG-SNR variation, depending on the type of speech being encoded, and the average SEG-SNR is around 15 dB. This objective quality is associated with an approximate mean opinion score of four, evaluated over a variety of operating conditions. This is broadly comparable to the quality of the 32 kbit/s CCITT G.721 ADPCM codec, to that of the seven-bit A-law or μ-law companded PCM codec, as well as to a 16 kbit/s SBC codec [11].
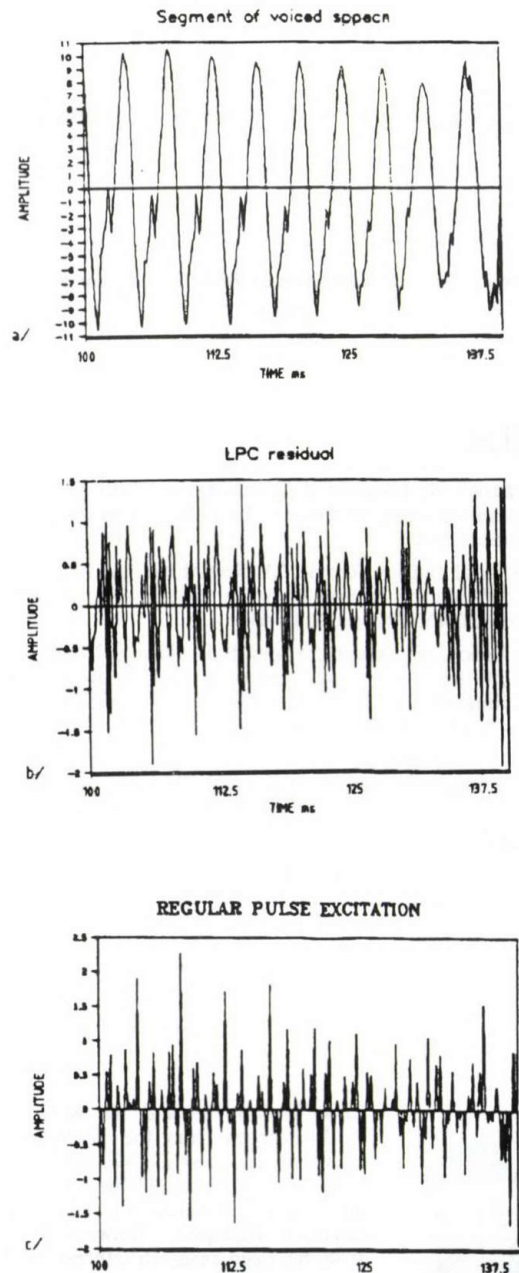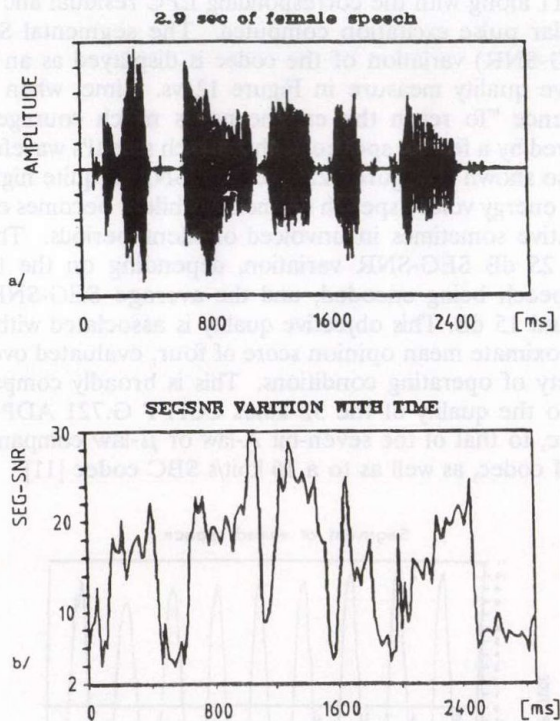

Figure 11. Characteristic waveforms of the RPE codec

2.9 sec of female speech

a/

b/

Figure 12. SEG-SNR variation of the RPE codec for a female speaker

8. SUMMARY AND CONCLUSIONS

With the advent of powerful floating-point DSP-chips and application specific integrated circuits (ASICs), high-complexity speech codecs, particularly analysis-by-synthesis hybrid codecs, are promoted from the status of pure academic interest to practical real-time schemes. On a somewhat more sober tone, however, their speech quality still has to be slightly compromised to mitigate computational complexity and hence power dissipation.

This process was demonstrated in the paper by describing the original high-quality, high-complexity RPE approach, and then simplifying it while slightly degrading speech quality to arrive at the standardised 13 kbps GSM-RPE codec. Informal listening tests using our simulated GSM-RPE codec showed only minor differences between the original and simplified RPE codec, while the complexity was reduced tremendously.

When used in a 16-QAM mobile radio system combined with embedded low-complexity binary Bose—Chaudhuri—Hocquenghem error correction codecs, the RPE codec showed remarkable robustness against channel errors and facilitated high-quality digital speech transmission in a bandwidth of around 10 kHz [10].

No, reduced computational complexity does not preclude high speech quality in RPE codecs, and as an additional bonus, high bandwidth efficiency and robustness is maintained.

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Lajos Hanzo received his M.Sc. and Ph.D. degrees from the Technical Univeristy of Budapest in 1976 and 1982, respectively, and since 1976 he has been with the Research Institute for Telecommunications in Budapest. Between 1976 and 1980, his main research interests included high-speed data transmission, digital filtering and modulation. From 1980 to 1981, he was on sabbatical leave working on parallel DSP modems at the University of Erlangen-Nürnberg in West Germany, while between 1981 and 1986, his research endeavours encompassed digital speech and data communications via satellites. In 1986 he joined the University of Southampton where he is teaching telecommunications. His recent research interest is the joint optimisation of source (speech, image, etc.) and channel coding as well as modulation schemes for dispersive fading mobile channels. Over the years he authored and co-authored some eighty scientific contributions and was awarded various distinctions.

News – Events

■ INTERNATIONAL WORKSHOP ON CHARACTERIZATION OF SEMICONDUCTOR SUBSTRATES AND STRUCTURES

The Workshop has been held in the Smolenice Castle (Czecho-Slovakia) from April 1st to the April 4th 1992. It has been organized by the Institute of Physical Electronics (Piestany, CSFR) and the Physical Section of the Union of Slovak Mathematicians and Physicists.

75 participants from Belgium, CSFR, France, Germany, Hungary, Italy, Japan, Poland, United Kingdom and the Ukraine presented their new results in the following areas:

- Defects in substrate;
- Thin layers and interfaces;
- Electrical characterization of substrates and structures.

The invited lectures, contributed papers and posters discussed mainly the characterization of GaAs, partly that of other III−V semiconductors and that of the silicon. The papers will be published in the near future in a special issue of the Journal of Crystal Growth.

The speakers of the Workshop pointed out, that as crystallographic defects can have a detrimental effect on the device performance its characterization and better understanding of defect formation mechanism is essential in the development of advanced Si-based ULSI-circuits and of III−V devices. Defect engineering which is now a new and rather exotic discipline in microelectronics will become therefore common practise in processing technologies to be used near the end of the century. ■

■ BOOK REVIEW

GRAPH THEORY, MATRICES AND FLOWS by B. Andrásfai

This book is the continuation of the first volume by the same author (Introductory graph theory − the same publishers, 1977). The first volume covered mostly such classical topics (trees, Eulerian and Hamiltonian walks, matching and extremal problems) which could be taught even at high school level. Indeed, since its first Hungarian language edition in 1971, it has had received very positive reviews, has had several editions, and was highly influential both in the postgradual training of Hungarian high school teachers and in the extracurricular activities of the more gifted high school students.

In the present volume the author addresses questions where some preliminary knowledge from undergraduate calculus is already desired.

The first chapter (Structure of the graph model) discusses the connected and 2-connected components of a graph, the strongly connected components of a directed graph and similar concepts. The second chapter (Optimal flows) covers such important topics as the optimal assignment problem, the single-commodity flows (including minimum cost flows) and the critical path problem.

Chapter 3 (Graphs and matrices) studies the various matrix descriptions of the graph (adjacency and incidence matrices, circuit and cutset matrices) and the interrelations among them. It covers the usual applications for the analysis of linear electric networks and also discusses in considerable details those areas of graph theory where the linear algebra properties of these matrices (especially the sprectrum of the adjacency matrix) have applications in pure graph theory.

The book is very clearly written, with many explanatory figures and examples. It also contains 128 problems with full solutions. It can be recommended as a textbook for those students of engineering, operations research or economics who wish to have a more advanced course in graph theory.

(Adam Hilger, Bristol − Publishing House of the Hungarian Academy of Sciences, Budapest (joint edition), 1990)

THREE PAN-EUROPAN EVENTS

EUROPEAN NUMBERING IN THE NINETIES — 11TH MAY 1992, LONDON, W1

The European Commission is funding a major study into the harmonisation of numbering throughout Europe. The first results of this research will be discussed at this major conference. Most countries in Europe are planning or have already made changes to their numbering system. There are manyu lessons to be learnt. Fred Gaechter himself will present the North American experience of numbering in a competitive environment, which will prove a very important case study to those involved in their own contry's numbering process.

CORDLESS COMMUNICATIONS CONFERENCE — 22ND JUNE 1992, LONDON, W1

This conference is a unique opportunity to compare and contrast the various regimes in Europe, and discover why Telepoint has so far proved more successful in the rest of Europe than in the U.K., why Norway is choosing GSM over any of the other offerings, what the current and projected penetration of cordless office products is across Europe and the U.S.A. and what sociological factors may inhibit the quick acceptance of cordless products.

SATELLITES FOR BUSINESS — 19TH MAY 1992 — OVERSEAS LEAGUE, LONDON, W1

Satellite communications have developed rapidly in Europe. It is now a year since the Green Paper was issued, and the single market is due to be complete by the end of the year. This timely conference will explain: the regulatory framework and its practical implications; applications in the U.K., Europe, and world-wide; the new mobile services; and networking by satellite. It will also explain the practical applications and the services, how they can bring added value and reduced costs to business operations.

To book for these conferences, please telephone our Conference Hotline on (071) 274 8725, or fax your booking form to (071) 733 0226, or (0908) 367281. Remember, the numbers if dialling from outside the U.K. are (+4471) 274 8725, (+4471) 733 0226 and (+44908) 367281

In the year 1992 we are continuing to publish the JOURNAL ON COMMUNICATIONS alternately in English and Hungarian, focusing each issue on a selected significant topic guest edited by an outstanding expert in the field. The planned issues are the followings:

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EUROPA TELECOM'92 – BUDAPEST

Telecommunication organizations world-wide are now rewriting their strategies to respond to the new guidelines and requirements created by the reshaping of Europe and its entrance into the European Economic Community. Europa TELECOM'92 Exhibition and Forum will be an integral part of this restructuring process.

THE EXHIBITION
Monday 12 – Saturday 17 October 1992

With approximately 16000 m^2 exhibition space planned for Europa TELECOM'92, it will be the largest regional show that has ever been produced. Exhibitors will be able to take full advantage of this abundance of space in order to demonstrate products and services with the minimum of restrictions. The duration of the exhibition will be six days in response to exhibitors' requests.

THE FORUM
Policy Symposium — Monday 12 – Wednesday 14 October 1992
Technical Symposium — Thursday 15 – Saturday 17 October 1992

Because the market in central Europe is so finely balanced, the Europa TELECOM'92 Forum will draw on the experience of the leaders from major telecommunication companies and policy makers shaping the technological boundaries of Europe.

A special Forum Advisory Council will help develop a Forum program that will address critical issues such as new legislations governing the installation of networks and equipment into the market, and how the developing countries will integrate these systems and source their equipment. The final program for this Forum will be issued closer to the event.

Information for authors

JOURNAL ON COMMUNICATIONS is published monthly, alternately in English and Hungarian. In each issue a significant topic is covered by selected comprehensive papers.

Other contributions may be included in the following sections:

- INDIVIDUAL PAPERS for contributions outside the focus of the issue,
- PRODUCTS-SERVICES for papers on manufactured devices, equipments and software products,
- BUSINESS-RESEARCH-EDUCATION for contributions dealing with economic relations, research and development trends and engineering education,
- NEWS-EVENTS for reports on events related to electronics and communications,
- VIEWS-OPINIONS for comments expressed by readers of the journal.

Manuscripts should be submitted in two copies to the Editor in chief (see inside front cover). Papers should have a length of up to 30 double-spaced typewritten pages (counting each figure as one page). Each paper must include a 100–200 word abstract at the head of the manuscript. Papers should be accompanied by brief biographies and clear, glossy photographs of the authors.

Contributions for the PRODUCTS-SERVICES and BUSINESS-RESEARCH-EDUCATION sections should be limited to 16 double-spaced typewritten pages.

Original illustrations should be submitted along the manuscript. All line drawings should be prepared on a white background in black ink. Lettering on drawings should be large enough to be readily legible when the drawing is reduced to one- or two-column width. On figures capital lettering should be used. Photographs should be used sparingly. All photographs must be glossy prints. Figure captions should be typed on a separate sheet.

For contributions in the PRODUCTS-SERVICES section, a USD 110 page charge will be requested from the author's company or insitution.